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DIs Inside

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Measure power-line distortion with a mixed-signal-THD analyzer

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Because of the performance of compressors and other inductive loads, it becomes more important to monitor the distortion on a power line. With alternative power sources, such as wind or solar, a distorted 60-Hz sine wave is more likely to be present. To measure this distortion, you can use a mixed-signal-THD (total-harmonic-distortion) analyzer to monitor the fundamental frequency amplitude and the second-, third-, fourth-, and fifth-harmonic content of the input signal. The analyzer, from Mixed Signal Integration (www.mix-sig.com) includes five bandpass filters and two op amps. The op amps provide gain and continuous-time filtering. The

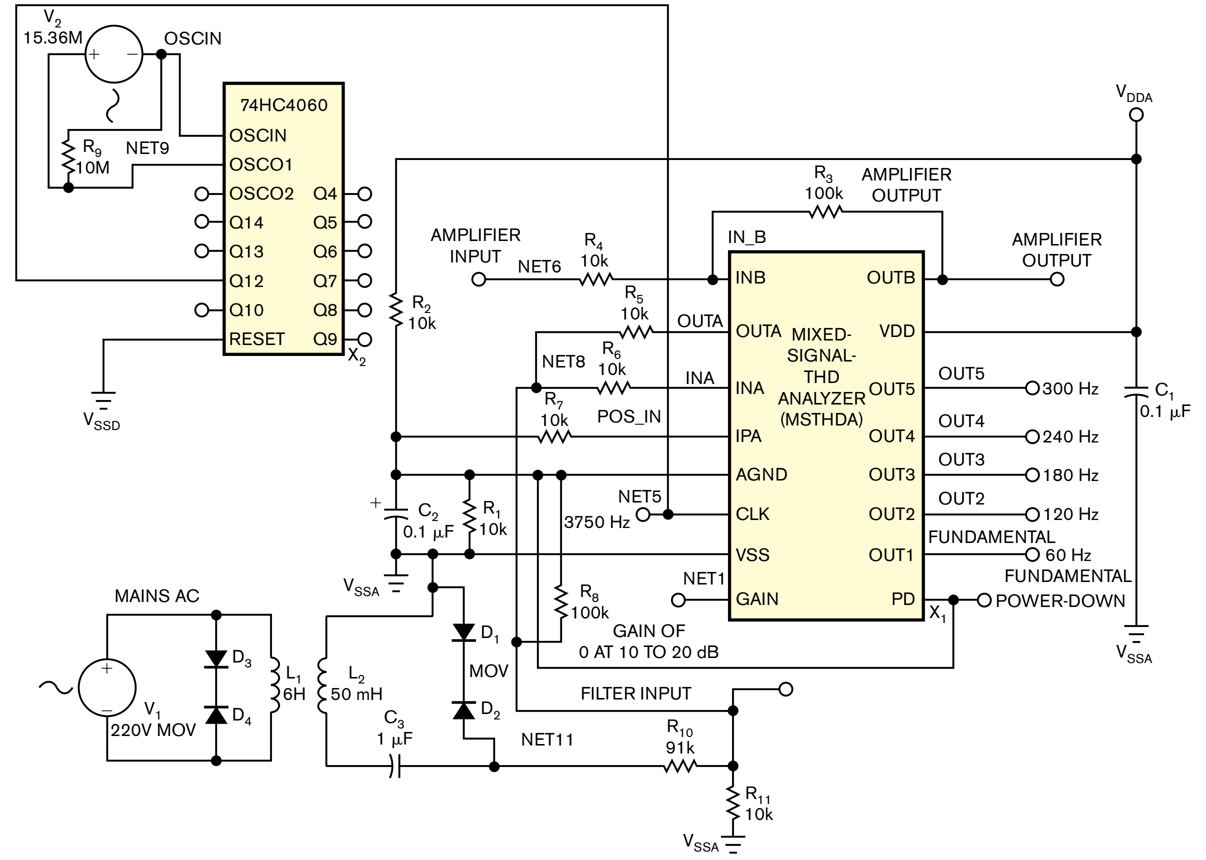

Figure 1 This mixed-signal-THD analyzer monitors the fundamental frequency amplitude and the second-, third-, fourth-, and fifth-harmonic content of the mains-input voltage.

analyzer also has digital-gain control for measurements in which the input amplitude is 10 or 20 dB lower than nominal: 2V p-p. The outputs of the analyzer are analog. Depending on the display that an application requires, you could tie the outputs to a bar-code interface, such as the LM3915 for 3-dB steps, or interface them with a multiplexer on a microcontroller for a digital readout.

Figure 1 shows the connections of the analyzer to the mains supply. A "wall-wart" transformer reduces the 120V mains voltage to 9V ac. This transformer provides 1500V isolation from primary to secondary and has low-distortion performance. The resistors in the divider act as fuses in case of a large surge voltage, and they reduce the voltage you apply to the analyzer. The back-to-back diode clamp protects the analyzer during momentary overvoltage conditions. In addition, a 220V MOV (metal-oxide varistor) across the transformer's primary protects the transformer. The analog ground centers on 2.5V and is derived from a 100-kΩ resistor-divider network. A 0.1-μF capacitor provides ac filtering. A 74HC4060 operates at 15.360 MHz; the divide-by-4096 (Q12) output connects to the analyzer's input-clock signal and supplies the clock for the device's switched-capacitor filters.EDN

Wireless "battery" energizes low-power devices

Carlos Cossio, Santander, Spain

Wireless connectivity is a growing trend in portable consumer gadgets. Unfortunately, designs cannot achieve true mobility because of short battery life, so the power cord still must connect the device to the power grid to get the required energy or to recharge the batteries. However, thanks to the low-power requirements of today's electronic devices, it is feasible to power them wirelessly. This Design Idea describes a simple approach to wirelessly transmitting energy to low-power devices at distances as great as 10 cm. This design uses the resonant-inductive-coupling principle working at 13.56 MHz. The system comprises the RF-power transmitter and the RF-power receiver.

Figure 1 shows the transmitter circuit, which incorporates a 13.56-MHz oscillator. The oscillator encompasses a CMOS 4069 inverter using power from a 9V battery to get a wide voltage swing. The oscillating signal then passes through a push-pull output stage comprising two small-signal MOSFETs to get enough current in the output coil. Finally, the output signal broadcasts to the outside by means of a serial-resonant-LC circuit incorporating a coil and a 60-pF variable capacitor tuned to 13.56 MHz.

Figure 2 shows the receiver circuit, which comprises an LC network tuned to a carrier frequency of 13.56 MHz. It includes a coil and a 60-pF variable capacitor in parallel with the coil. A full-bridge rectifier comprising four 1N4001 diodes rectifies RF power. Rectification efficiency is approximately

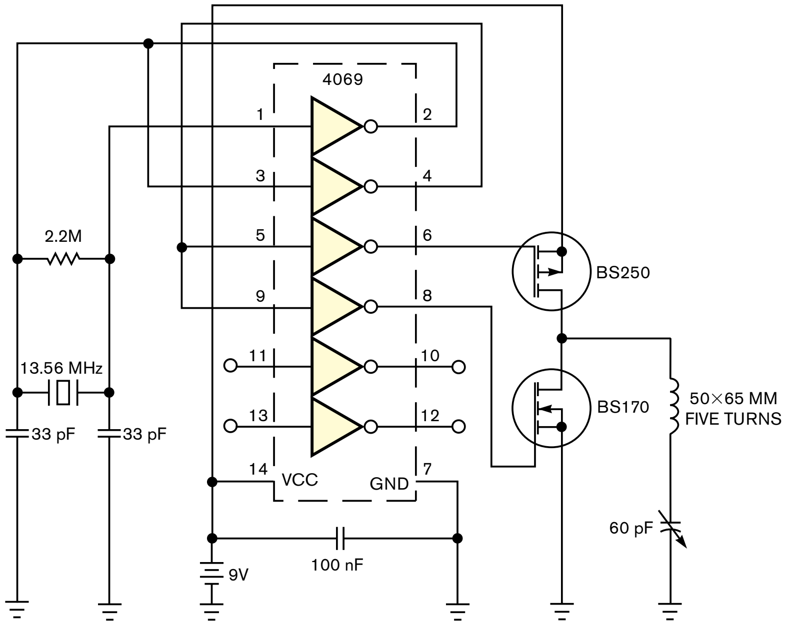

Figure 1 A simple 13.56-MHz oscillator energizes an antenna coil, broadcasting power to the receiving circuit in Figure 2.

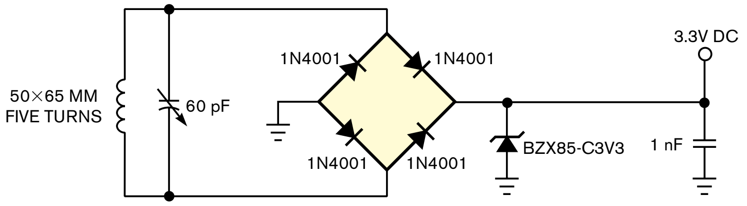

Figure 2 This receiver rectifies the signal from the oscillator in Figure 1, powering low-current consumer gadgets.

50%. Reaching 3.3V of output voltage requires a 9V p-p ac voltage across the coil's pins. A shunt regulator incorporating a 3.3V zener diode provides voltage clamping beyond 3.3V to prevent power-level variations with distance. Finally, a 1-nF capacitor after the full-bridge rectifier decouples the power supply. The two coil antennas use five turns of 1-mm enameled-copper wire in a rectangular, 50×60-mm shape.

As an improvement, if your application requires greater distance, you can increase the power supply to 15V to get a greater voltage swing on the transmitter coil, thanks to the CMOS technology the oscillator design employs. In addition, designing a larger-coil antenna in the transmitter and the receiver sides helps to increase the distance of operation. **EDN**

Solid-state analog-data recorder runs for 7.4 days

S Vinay Kumar, Mysore, India

The solid-state data recorder in **Figure 1** can continuously record the temperature for approximately 178.42 hours, or 7.434 days. The LM-35DZ transducer converts the temperature to an analog-voltage equivalent. The analog voltage then goes to the HI5812 ADC, and the digital data gets stored in the nonvolatile DS1270W SRAM at a rate of 3.265 samples/sec. To retrieve the analog signal, the digital data in memory goes to the DAC08. The output of the DAC then goes to the current-to-voltage converter, then to analog switch MC14066, and finally to the output buffer. The address generator is a simple counter, the MC14040. A record-and-play circuit uses an MC14049, and analog switches control the read and write states of the nonvolatile SRAM. A 10-kΩ potentiometer sets the reference voltage of both the ADC and the DAC.

Pressing and releasing the reset button once causes the recording or playing to start from the beginning of the memory location; the recording or playing function depends on the position of the record-and-playback switch. If you close the record-and-playback switch, recording takes place; if the switch is open, playing occurs. **EDN**

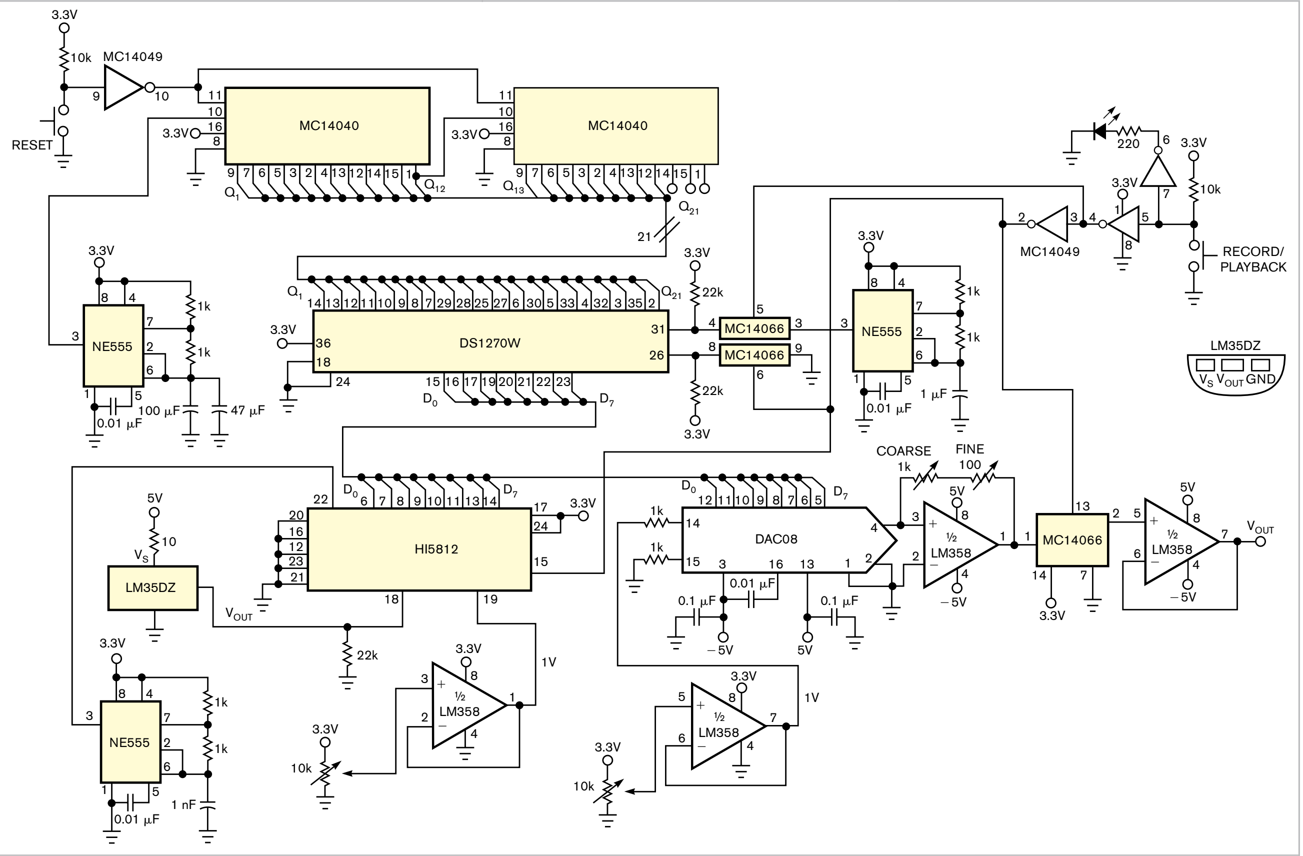

Figure 1 This solid-state data recorder uses an ADC to digitize data, which gets stored in a nonvolatile SRAM. To read back the analog data, the memory's contents shift to a DAC, depending on the state of the record-and-playback switch.

Wideband peak detector operates over wide input-frequency range

Jim McLucas, Longmont, CO

This Design Idea builds on a previous one (**Reference 1**) to realize a precision peak detector with a bandwidth of 15 to 30 MHz or more, depending on the maximum input-signal level of your application. The crucial feature of this Design Idea is an ultrafast comparator that provides the high slew rate and low propagation delay that this application requires. The comparator in this design is the Analog Devices (www.analog.com) AD8561, a 7-nsec device (**Reference 2**). This peak detector provides accuracy from 100 Hz to more than 14 MHz at input-signal levels of 100 mV p-p to 6V p-p. At higher frequencies, the maximum usable input-signal level decreases. The circuit exhibits an accuracy of ±3% over much of the input-level range. Also, its high input impedance of about 100 kΩ in parallel with 3 pF does not significantly load the circuit under test in many applications; 3 pF results in an impedance of 3.5 kΩ at 15 MHz.

Referring to **Figure 1**, the high-input-impedance buffer comprising IC$_1$ and its associated components provides the ac signal to the ultrafast comparator, IC$_3$. The output of IC$_1$ centers on 0V dc by the action of op amp IC$_{2A}$ and its associated components, which sample the dc level at Pin 6 of IC$_1$ and then provide a dc-correction voltage to Pin 3 of IC$_1$. This action virtually eliminates the effects of IC$_1$'s input-offset voltage and input-bias currents. R$_1$, R$_4$, and C$_1$ provide a small amount of gain boost as the frequency increases to 25 MHz, and C$_5$ then begins to roll off the gain.

The input signal capacitively couples to the input buffer, so, for proper operation, the input-ac signal must have a symmetrical waveform, such as a sine wave. An unsymmetrical waveform has a shift in its peak value after passing through C$_2$, and, as a result, the output of the peak detector will be inaccurate.

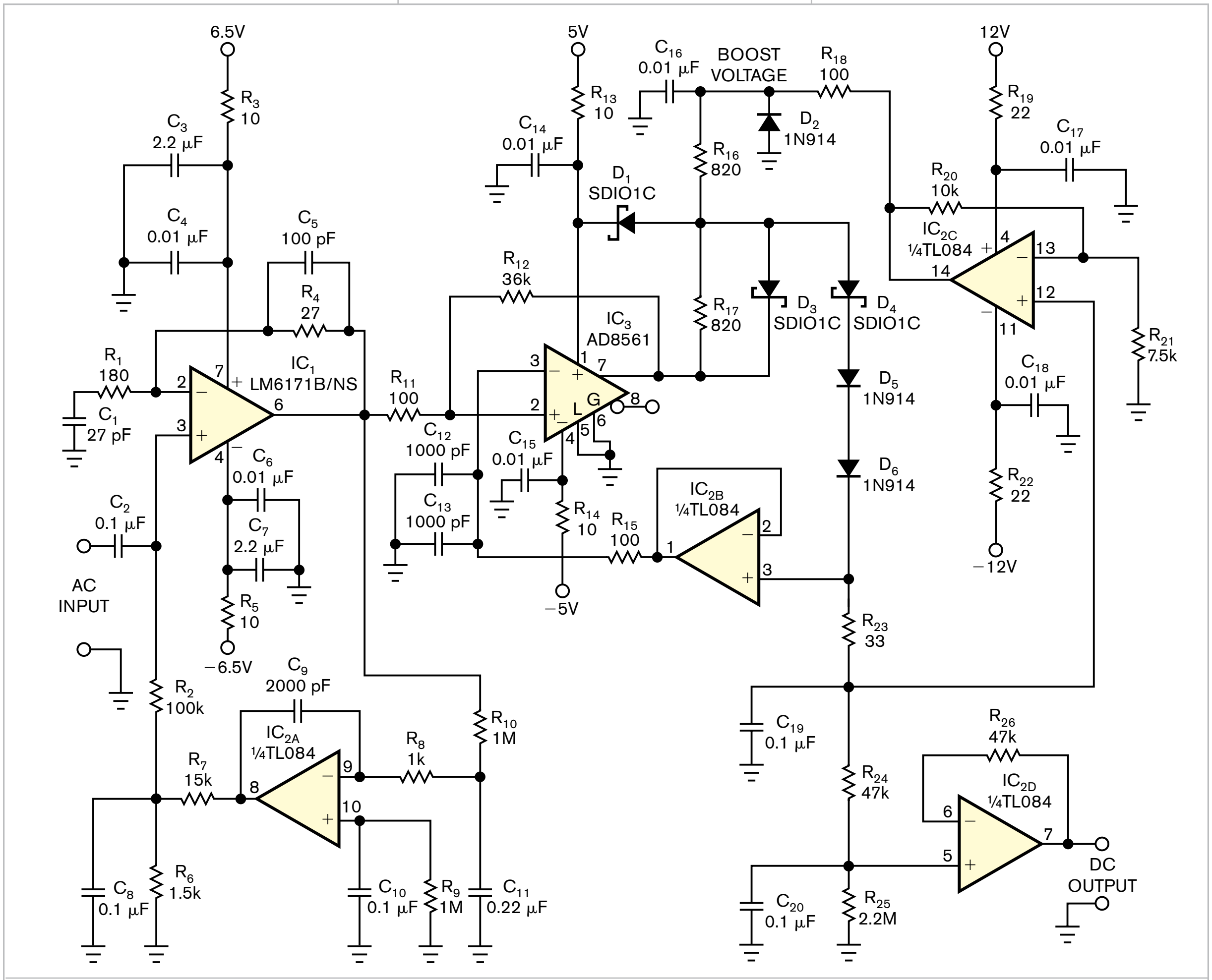

Figure 1 This precision peak detector uses an ultrafast comparator to achieve high accuracy over a wide input-frequency range.

The output of comparator IC_3 swings high when the input at Pin 2 is higher than the dc level at Pin 3. This action, in turn, charges holding capacitor C_{19} through R_{17}, D_4, D_5, D_6, and R_{23}. When the voltage on C_{19} is higher than the peak signal level at Pin 2 of IC_3, the comparator stops providing charging pulses at its output. At equilibrium, the comparator provides output pulses with the correct amplitude and width to maintain the voltage on C_{19} at approximately the peak level of the input signal. The high-input-impedance dc buffer, IC_{2B}, minimizes the discharging of C_{19} between charging pulses.

The network comprising R_{24}, R_{25}, and C_{20} filters and attenuates the dc output by 2.1%. This attenuation is necessary because the output tends to be slightly higher than the actual peak level of the input signal at Pin 3 of IC_1. The circuitry comprising IC_{2C} and its associated components provides a novel feature: a voltage boost at Pin 14 of IC_{2C} as the voltage on holding capacitor C_{19} increases. The circuitry then applies this voltage boost to R_{16}, which in turn causes the voltage swing at the junction of R_{16} and R_{17} to increase as the charge on C_{19} increases. This action causes the amplitude of the pulses driving D_4 to increase. This action maintains a relatively constant drive to C_{19} as its charge increases.

Diode D_1 keeps the voltage at the output of IC_3 from exceeding its supply voltage. Diode D_2 keeps the boost voltage from going to a large negative level at start-up, which could cause the circuit to latch up. The switching action of the comparator and diode D_3 prevents latch-up due to a large positive-boost transient. This circuit exhibits no indication or tendency for instability. The maximum input signal is 6V p-p because of the input common-mode-voltage specification of the AD8561 comparator. The supply voltages for the input buffer are ±6.5V to avoid the possibility of severely overdriving the comparator.

You can improve the precision of the circuit by substituting a 100-kΩ potentiometer for R_4 to provide an output-level adjustment, and a dc-offset adjustment would improve accuracy at low signal levels.

This circuit used a 300-MHz-bandwidth oscilloscope to make the performance measurements. As a result, the data in **Table 1**, which is available in the online version of this Design Idea at www.edn.com/071122di1, may include some measurement errors. Therefore, take the results in the **table** as representing the circuit's performance rather than as precise data. The data is simply the result of the best equipment on hand when the measurements were made.**EDN**

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1. McLucas, Jim, "Precision peak detector uses no precision components," *EDN*, June 10, 2004, pg 102, www.edn.com/article/CA421510.
2. "AD8561 ultrafast 7 ns single supply comparator," Analog Devices, www.analog.com/UploadedFiles/Data_Sheets/AD8561.pdf.