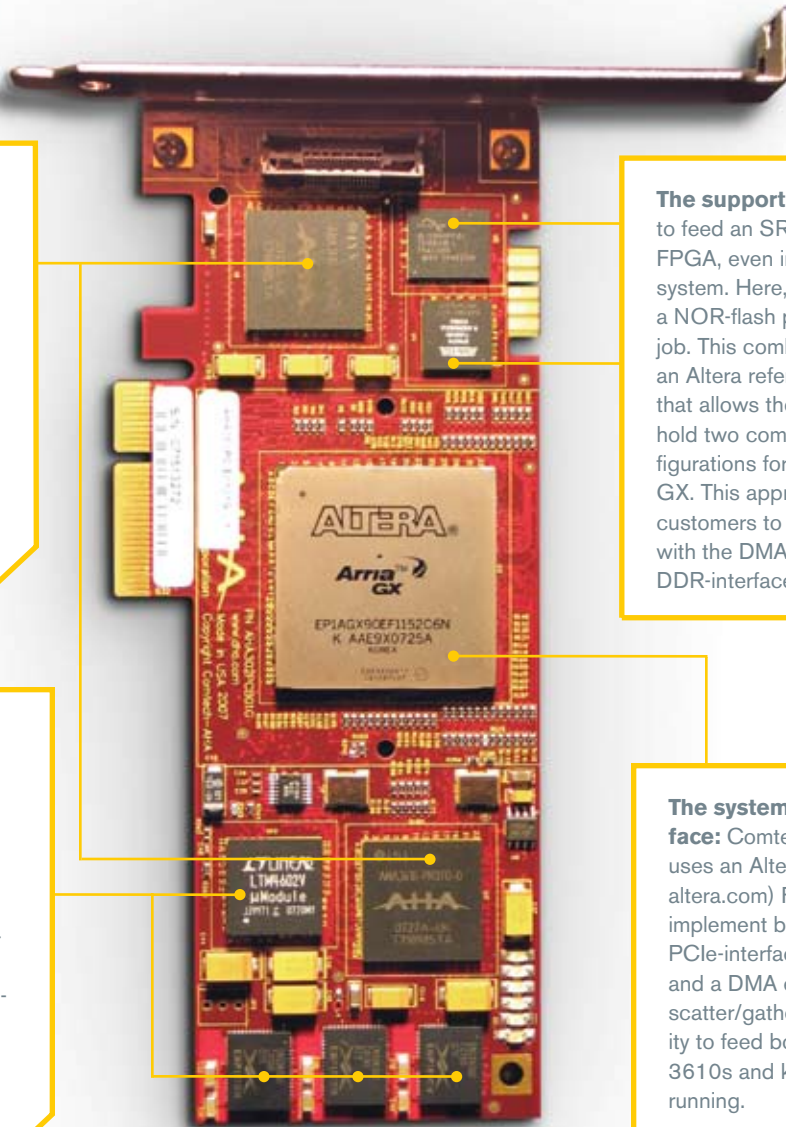


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Plugging hardware-based compression into a server

Lossless data compression can be valuable in any number of storage, server, and networking situations, reducing both required bandwidth and storage space without damaging the data. It's too laborious to achieve high throughput in software using the Lempel-Ziv-type algorithms necessary for good compression ratios. One vendor, Comtech AHA Corp (www.aha.com), plans to offer a drop-in PCIe (PCI Express) card as a hardware accelerator for the open-source gzip (GNU-zip) algorithm. The board will be available in the first quarter of 2008, but the company offered *EDN* an early look at what it takes to accelerate gzip.



The crunchers: The AHA 3610s are numerical processors that do the gzip computations. Using internal buffer memory, they can work directly from the host server or the PC's main memory. The data interface is a parallel pair of 16-bit DDR-DRAM interfaces, allowing each chip to compress or decompress data at 2.5 Gbps, with the equivalent of gzip-9 (high-effort) software-compression results.

The support: You have to feed an SRAM-based FPGA, even in a small system. Here, a CPLD and a NOR-flash part do the job. This combination is an Altera reference design that allows the board to hold two complete configurations for the Arria GX. This approach allows customers to experiment with the DMA logic and DDR-interface control.

The power: A Linear Technology (www.linear.com) switching dc/dc converter steps down the 12V supply from the PCIe connector to 3.3V for three Enpirion (www.enpirion.com) buck regulators, which in turn provide 2.5V for SSTL (stub-series-terminated-logic) I/O and 1.2V for core logic to the FPGA and Comtech AHA chips.

The system interface: Comtech AHA uses an Altera (www.altera.com) FPGA to implement both the PCIe-interface logic and a DMA engine with scatter/gather capability to feed both the 3610s and keep them running.