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## Protect yourself

**T**his installment of “Analog Domain” focuses on one of the growing circuit-implementation challenges that confronts IC, subsystem, and system designers alike: interface ESD protection. Two trends make interface protection increasingly difficult as we move along our industry’s current technology trajectory. First, increasing demands for processing speed and functional density have pushed IC fabricators to shrink

further the minimum dimensions of MOS devices. For a given gate dielectric, device physics require maintaining the dielectric thickness in proportion to lateral dimensions (Reference 1). Thinner dielectrics, however, are more susceptible to ESD overstress.

Second, port speeds continue to increase, particularly with the growing success of portable-media devices. As one example, the 1996 USB 1.0 release provided for 12-Mbps interfaces. Four years later, a USB 2.0 feed could reach 480 Mbps. The yet-unreleased USB 3.0, shown at this year’s Intel Developer Forum, trades copper interconnect for parallel fiber-optic cable to attain a 4.8-Gbps connection. IEEE 802.3 (Ethernet) and IEEE 1394 (Firewire) show the trend to a greater or lesser degree.

Traditionally, ICs include ESD-shunting structures within their standard interconnect-pad cells, which protect the internal circuitry from ESD strikes to the device’s pins. The on-chip-ESD protection may be all that’s necessary to see an IC safely from its manufacturer to a board assembler if both organizations adhere to strict anti-ESD-handling procedures. Though on-chip-ESD structures serve as excellent *secondary* protection, however, they are usually insufficient to protect

an interface over years of exposure in uncontrolled environments.

The reasons these structures are insufficient are twofold: They are too small to absorb large energy transients that interfaces commonly experience in the field, and they reside too far away from the interface-entry point to prevent coupling to adjacent traces. Once an I/O line’s on-chip-ESD cell begins to conduct, a current transient develops along its trace, exciting the trace’s inductance, causing a corresponding voltage transient,  $Ldi/dt$ . Adjacent conductors with mutual inductance to the I/O trace see coupled transients that can exceed the capabilities on their own on-chip-ESD cells. These adjacent traces can include clock, data, or other nonported signals (Reference 2).

Mounting TVSs (transient-voltage suppressors) as close to the entry point as possible alleviates this problem by shunting the ESD event to ground before transient currents develop inside your product. Doing so can add substantially to your product’s robustness with minimal additional cost. “If a finger can get close to a node, protect it,” is a good rule of ... errrrr ... thumb. This rule applies to keypad switch lines, too, despite their insulating keycaps.

High-speed interfaces require TVSs with particularly low shunt capacitances. Check your vendor’s product line for devices built for specific high-speed interfaces. If you don’t find devices specifically for your interface, compare your signaling frequencies and source-and-line characteristics with those of interface standards that the vendor explicitly supports. When considering TVS manufacturers’ claims, be sure to understand which ESD source model they use when specifying their devices. The JEDEC HBM (human-body model), for example, uses a 100-pF capacitor discharging through a 1.5-k $\Omega$  resistor. The repeatability of the test method’s results has been historically an area of concern (Reference 3). The IEC-61000-4-2 standard’s test method promotes repeatability, and its source model—150-pF behind 150 $\Omega$ —is more demanding of your design. **EDN**

### REFERENCES

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