



BY BONNIE BAKER



Delta-sigma ADCs in a nutshell

Delta-sigma converters are ideal for converting signals over a wide range of frequencies from dc to several megahertz with very-high-resolution results. **Figure 1** shows the basic topology, or core, of a delta-sigma ADC, which has an internal delta-sigma modulator in series with a digital filter. As you explore delta-sigma ADCs, you will find that, although they have a variety of other features, they all possess this basic structure. This column and the next three *Baker's Best* columns explore the basic topology and functions of these two modules.

The input signal to the delta-sigma ADC is an ac or dc voltage. This and the next three *Baker's Best* columns use a single cycle of a sine wave as the input signal. Using a 1-bit internal ADC, the internal converter modulator in **Figure 1** samples the input signal, producing a coarse, quantized output. The modulator converts the analog-input signal into a high-speed, pulse-wave representation. The ratio of ones to zeros in the modulator's output pulse train mirrors the input-analog voltage. Although the

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modulator produces a noisy output, future columns will show that the circuit "shapes" this noise into the high-

er frequencies of the output spectrum. This action paves the way for a low-noise, high-resolution conversion at the output of the digital filter.

At the modulator output, the digital filter addresses high-frequency noise and high-speed-sample-rate issues. Because the signal now resides in the digital domain, you can apply a lowpass digital filter to attenuate the higher frequency noise and a decimator filter to slow down the output-data rate. The digital/decimator filter samples and filters the modulator's stream of 1-bit codes and creates a slower multibit code.

Although most converters have only one sample rate, delta-sigma converters have two: the input sampling rate and the output-data rate. The ratio of these two meaningful variables defines the system's decimation ratio. A strong relationship exists between the decimation ratio and the converter's effective resolution. A future column will examine how the modulator, digital/decimator filter, and adjustable decimation ratio work. **EDN**

REFERENCE

1 Baker, R Jacob, *CMOS Mixed-Signal Circuit Design: Volume II*, John Wiley & Sons, 2002, ISBN: 0471227544.

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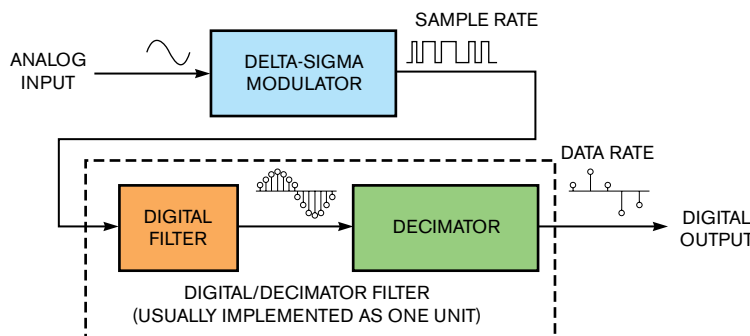


Figure 1 The core functions inside any delta-sigma ADC are a delta-sigma modulator and a digital/decimator filter.

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