Actively driven ferrite core inductively cancels common-mode voltage

W Stephen Woodward, Chapel Hill, NC

An earlier Design Idea illustrated one approach to that traditional headache for the analog designer: the dreaded ground loop (**Reference 1**). That Design Idea described a simple and efficient multichannel circuit. But it's an asymmetrical CMV (common-mode-voltage) approach in that it works only at the receiving end of a cable. It therefore applies only to signal inputs and does nothing for outputs. However, in cases in which CMV consists of purely ac noise, a different CMV-remediation method—active inductive cancellation—works bidirectionally and therefore cancels CMV-error components in both input and output signals.

Engineers have for many years used passive-CMV inductive cancellation (**Figure 1**). Sometimes called a "humbucker transformer" because the power mains' 60-Hz "hum" is often a dominant CMV component, the CMV inductor comprises a primary winding in series with the ground connection between the signal source (1) and the destination (2) and a secondary winding with a 1-to-1 turns ratio.

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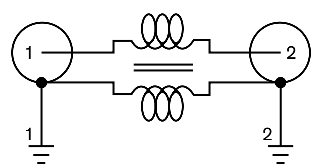

Figure 1 In the classic humbucker configuration, the CMV inductor comprises a primary winding in series with the ground connection between a signal source (1) and a destination (2) and a secondary winding with a 1-to-1 turns ratio.

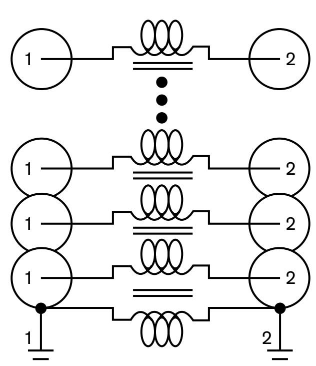

Figure 2 You can extend the passive approach in Figure 1 to multiple channels at the expense of a large magnetic component.

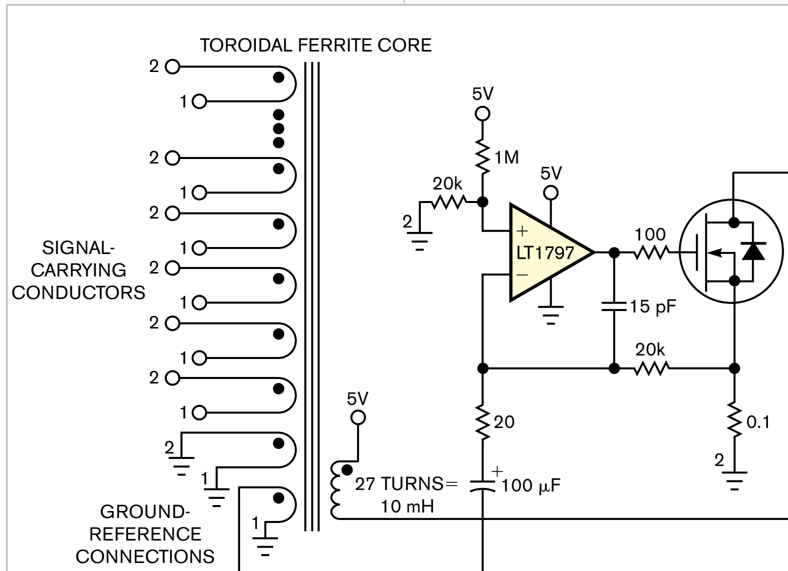

Figure 3 Using the active drive of the CMV core, you can achieve CMV reduction of 40-dB or more cancellation, extending from tens to millions of hertz.

The principle of the CMV transformer relies on magnetic coupling between the primary and the secondary, such that any voltage that appears across the primary induces an equal and opposite voltage in the secondary, thus canceling it. You can easily extend the principle to multiple signal channels simply by adding more secondary windings—one secondary for each channel (**Figure 2**).

However, the Achilles' heel of the CMV transformer is the fact that the decibels of cancellation fall off at the low-frequency end of the noise spectrum. This situation occurs because noise cancellation depends on the fact that the inductive reactance of the windings must be much larger than the impedance of the cable. Hundreds of millihenries of inductance are necessary to satisfy this criterion for frequencies as low as 60 Hz. For multichannel applications requiring cancellation for frequencies as low as 60 Hz, this fact translates to lots of copper, core, bulk, and weight. However, if you don't mind if your designs consume a little power, then a work-around exists: actively driving the CMV core.

In **Figure 3**, the power amplifier comprising the LT1797 high-frequency op amp and MOSFET forces the driven core to precisely cancel CMV as sensed in the ground-reference connection. The result is such a large multiplication of the apparent winding inductance that you can reduce the "windings" to a simple single pass-through of the toroid core. In other words, you need to thread a multiconductor-signal cable only once through the "hole in the doughnut" to achieve CMV of 40-dB or more cancellation, extending from tens to millions of hertz. EDN

REFERENCE

[1] Woodward, W Stephen, "Amplifier cancels common-mode voltage," *EDN*, May 10, 2007, pg 82, www.edn.com/article/CA6437955.

Improved optocoupler circuits reduce current draw, resist LED aging

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It seems deceptively simple to establish galvanic isolation with the help of optocouplers between circuits that operate at different ground potentials. Optocouplers draw power from the isolated circuit, and switching can be relatively slow and uncertain because of LED aging. Substitutes without optocouplers, such as the ADUM12xx from Analog Devices (www.analog.com) or ISO72x from Texas Instruments (www.ti.com), are available. This Design Idea describes a method of improving the simple optocoupler.

Figure 1 shows two popular designs of 0V synchronization with ac. An attempt to reduce power draw from the isolated circuit by decreasing the optocoupler's LED current with a corresponding increase of the optocoupler's load resistor yields slower and more uncertain switching. To achieve faster and sharper switching, you would have to sacrifice power efficiency; however, the benefit of this sacrifice is limited because of the inverse relationship between power efficiency and the ac-voltage magnitude.

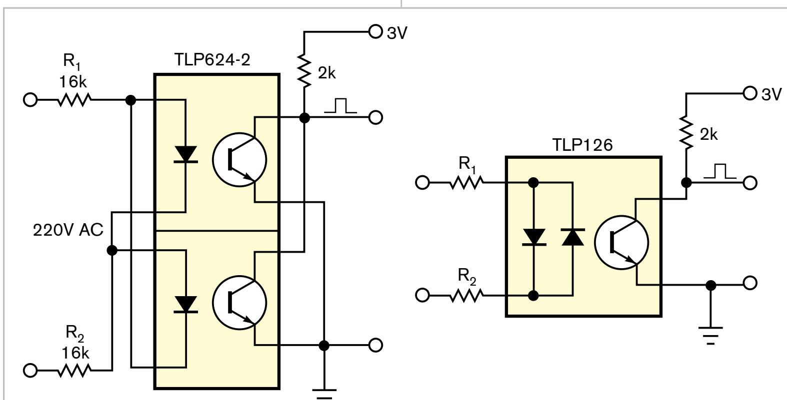

Figure 1 Establishing galvanic isolation with the help of optocouplers between circuits that operate at different ground potentials looks deceptively simple. Optocouplers draw power from the isolated circuit, and switching can be relatively slow and uncertain because of LED aging.

An optocoupler's LED emits almost continuously during nearly all ac cycles exceeding the nominal, leading to low power efficiency and relatively fast aging of the optocoupler. One more drawback is excessively large and nearly uncontrollable zero-crossing error; the circuit's sensitivity threshold depends on the parameters of the optocoupler. The designs in **Figure 1** do not provide an ideal approach. With respect to efficiency, they can draw 5 to 100 mA, depending on the optocoupler's current-transfer ratio and the ac amplitude.

The design in **Figure 2** overcomes the problems of excessive power consumption, uncertain switching, and LED aging. It lends itself well to wide-ac-range applications. Compared with the circuit in **Figure 1**, **Figure 2**'s LED emits only in close vicinity of the zero-crossing point and receives its power from the previously charged capacitor, so you can reduce the average current draw by a factor of 10 to 100. The design also provides faster, more

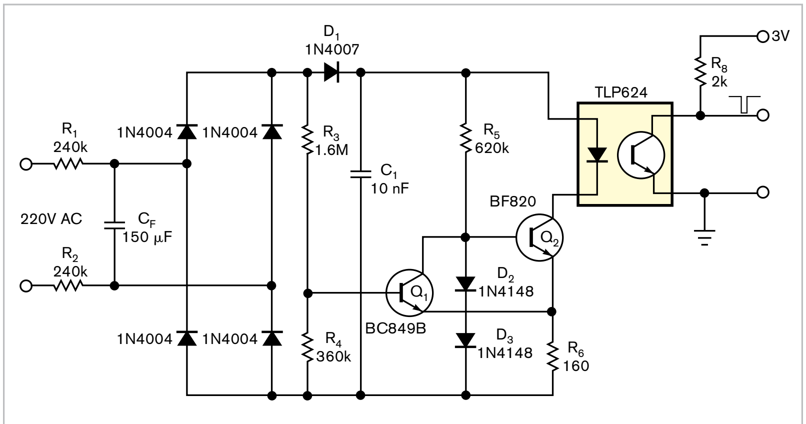

Figure 2 This circuit overcomes problems of excessive power consumption, uncertain switching, and LED aging.

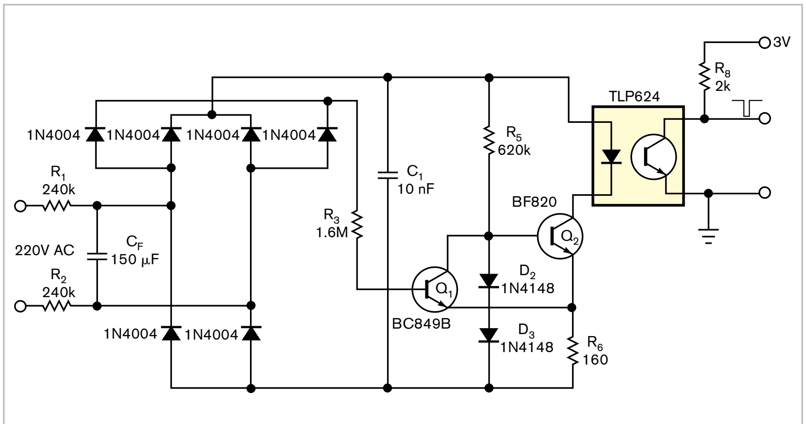

Figure 3 Another variant of this design shows how to manage without a requirement for minimal reverse current in D_1.

deterministic, and sharper switching. What's more, you can expect slower LED aging. Resistors R_1 and R_2 in **Figure 1** dissipate no less than 1.5W of power as waste heat, so changing them to 0.1W devices allows placement of additional components on the same board area (**Figure 2**).

The circuit's main components comprise amplitude detector D_1, capacitor C_1, and Schmitt trigger Q_1/Q_2 to control a current through the optocoupler's LED. D_2 and D_3 stabilize the base voltage of Q_2 and, hence, its collector current, which activates the optocoupler. Capacitor C_1 charges up through R_1, R_2, and D_1.

During nearly all of the ac-cycle time, except in the vicinity of the zero-crossing point, Q_1 is on, and Q_2 is off. Then, approaching the zero-crossing point, the state of Schmitt trigger Q_1 and Q_2 changes, and Q_2 discharges capacitor C_1 with the constant current, because the circuit comprising Q_2, D_2, D_3, R_5, and R_6 stabilizes current as $I=(2\times V_D-V_{BE2})/R_6$, where V_D is the voltage drop on D_2 or D_3 and V_{BE2} is the base-emitter voltage of Q_2.

Some applications require none of the hysteresis that is inherent to a Schmitt trigger; **Figure 3** shows such a design. It also shows how to manage without a requirement for minimal reverse current in D_1. This circuit, however, better suits pure synchronization and not thyristor control. Because of the stability of LED current, these designs provide an expanded input-ac-voltage range, which may be useful for a multistandard ac-powered gadget; an opportunity to set the LED current without the risk of overloading the LED; and a reduced influence of the optocoupler's instability. One more advantage of these designs is their inherently safer nature. In the case of a short circuit in their terminals, optocouplers deliver 10 to 100 times less current between the isolated and the nonisolated sides than the circuit in **Figure 1**. The optocoupler also offers advantages. Thanks to the low duty cycle, you can freely reduce the value of the optocoupler's load resistor, R_8, without sacrificing power efficiency. This reduction results in low zero-crossing error. EDN

Cascade two decade counters to obtain 19-step sequential counter

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This Design Idea offers a practical approach to cascading two or more Johnson counters together with a bare minimum of parts. The CD4017 Johnson decade counter finds use in simple circuits ranging from sound effects to LED displays. The counter's outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. The dc-supply voltage can range from approximately 3 to 18V dc. The dc-current drain per each output pin (Q0 to Q9) is 10 mA. The circuit has passed tests at 12V dc at 0 to 150°F without anomalies.

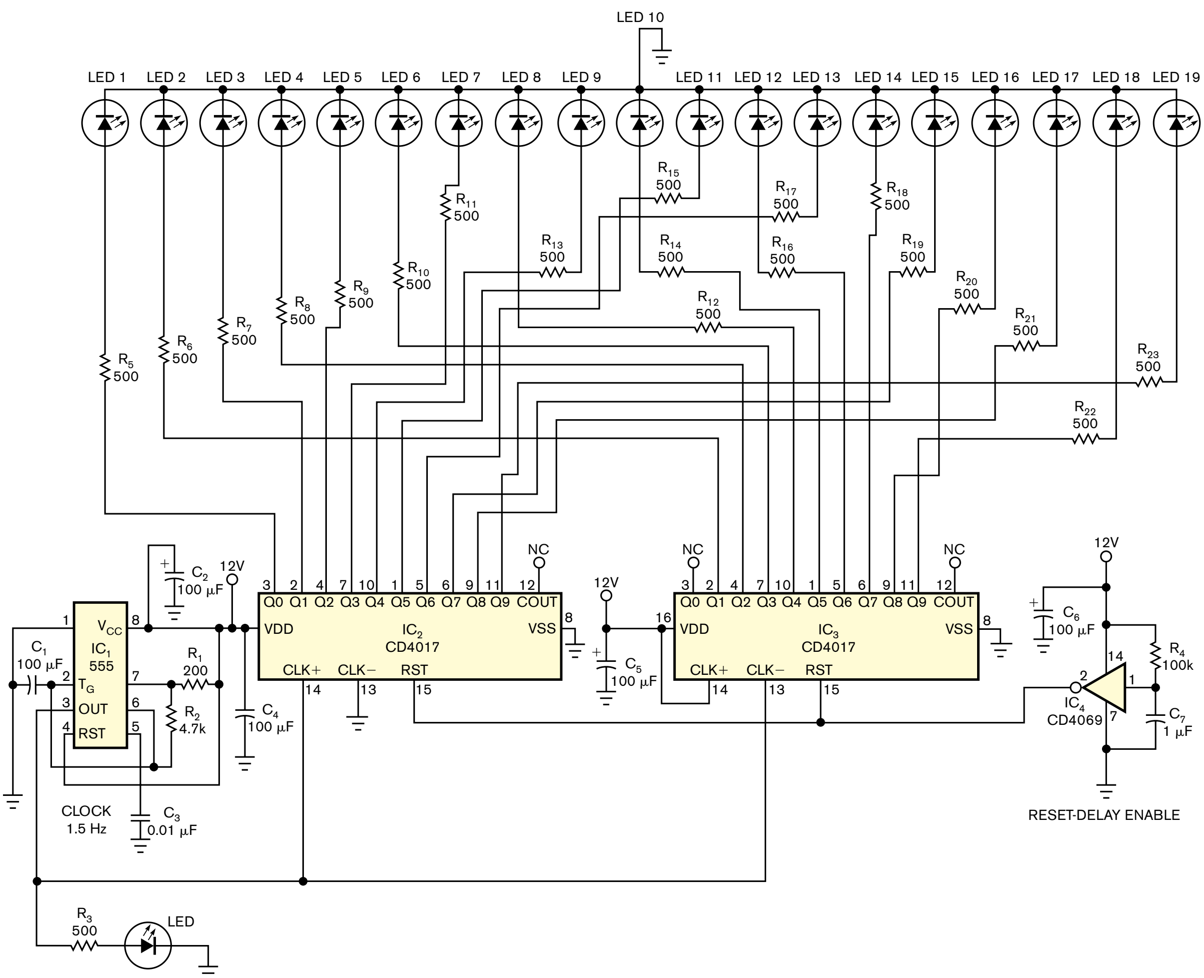

Figure 1 By interleaving the outputs of two cascaded CD4017 Johnson counters, you can obtain a 19-step sequential output.

The circuit in **Figure 1** uses only four ICs and yields a 19-step sequential count. You cannot get 20 outputs without adding more hardware because of the fact that, upon powering up, each CD4017 counter displays output Q0 as being on. Therefore, the circuit does not use output Q0 of IC_3 and can use only 19 of the 20 outputs.

At first blush, you might think that you could simply cascade two counters together using the carry-out pin, Pin 12, from one counter to feed the clock-input pin, Pin 14, of a second counter. But the problem with this configuration is that it does not provide sequential count from 1 to 20 because the first counter begins to count over again once it has reached 10. Such a configuration is a zero-to-99 counter because every 10 counts on the first IC counter causes one count on the second IC counter.

By hooking together two counters, you can obtain a sequential count from 1 to 19. The circuit uses IC_4, a CD4069 inverter, as a reset-delay enable to cause a few milliseconds of delay before each counter can begin to count. A high signal on the Pin 15 Reset clears the counter to its zero count.

Without the delay time, each counter powers up with a random output count such that several LEDs may be on. The circuit uses IC_1, a 555 timer, as the clock to generate a 1.5-Hz square wave. You can change the frequency by changing the RC time constant comprising R_1, R_2, and C_1. Keep in mind that, to obtain a 50% output duty cycle, make R_2 much larger than R_1. Pin 14 of IC_2 has a positive-edge clock trigger. Pin 13 of IC_3 has a negative-edge clock trigger. Therefore, when the clock goes high, IC_2 produces an output count. When the clock goes low, IC_3 produces an output count. By interleaving the outputs, you obtain a sequential count from 1 to 19. Because each clock cycle has both a high and a low state, after the first clock pulse, two LEDs will always be on—that is, LED 1, LED 1 and 2, LED 2 and 3, LED 3 and 4, and so on. Go to www.edn.com/071214di1 to see a short video clip of the finished circuit in action. EDN

Dual-input sample-and-hold amplifier uses no external resistors

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At least two classic ways exist to address applications requiring sampling of a sum of analog voltages. The most common way is to cascade a classic analog adder and a sample-and-hold amplifier. A classic analog adder is an op amp plus at least three precision resistors. The values of these resistors should be as low as possible so as not to deteriorate the bandwidth of the adder. On the other hand, such low-value resistors dissipate power. Further, the configuration of an adder-sample-and-hold amplifier suffers also from another drawback, which manifests itself when the two input voltages are close in magnitude but of opposite polarity. In this case, even if the magnitude of the input voltages is high, the resulting sum is low or no voltage if the magnitudes of input voltages are equal. Sampling a low voltage usually involves a high relative error of the output voltage because each amplifier has some dynamic errors, such as residual parasitic transfer of charge into the storing capacitor.

Another possibility is to use one amplifier per channel and add their outputs in a classic analog adder. Although this configuration avoids the problem with the high relative error of output voltage when input voltages are similar in magnitude and opposite in polarity, precision resistors in the adder still dissipate power.

You can avoid these problems by using the circuit configuration in **Figure 1**, which uses no external resistors. In the steady state, the internal-tracking interval, the $\overline{Q}_D$ internal-logic signal is at an active-high level, enabling the A_1, B_1, and A_2 followers. Thus, the ground-referenced capacitor, C_2, charges to the V_{INA} voltage. The lower node of capacitor C_1 at Pin 2 of IC_2 gets temporarily grounded through the out-

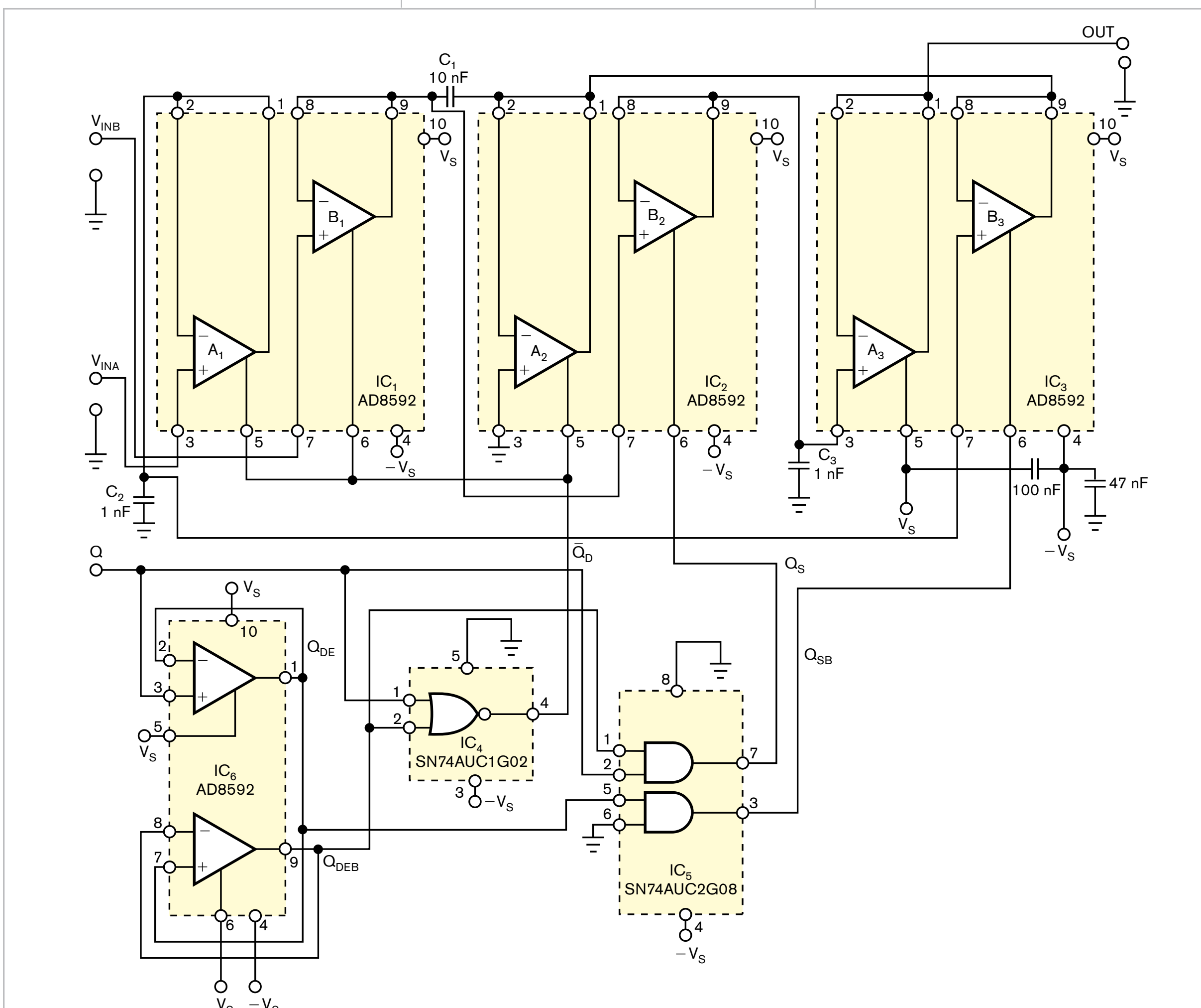

Figure 1 The basis of the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on the C_2 and C_1 capacitors, stacking these capacitors within the sample interval, and storing the value of stack's voltage on the C_3 capacitor.

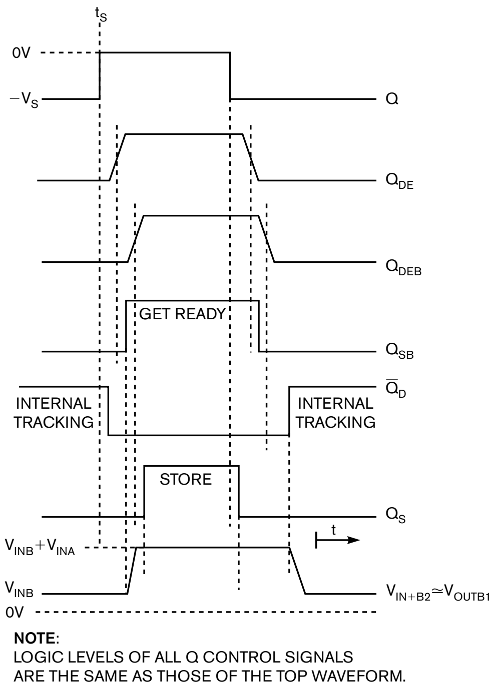

Figure 2 The bottom waveform shows that, at the upper node of the C_1 capacitor, the V_{INB} voltage appears within the tracking interval, and it rises to the value of the sum of both input voltages within the get-ready interval.

put of the A_2 follower while it charges to the V_{INB} voltage at its upper node at Pin 9 of IC_1. V_{INA} and V_{INB} are the input voltages at the A and B inputs, respectively.

After a settling period, when all internal logic-control signals are low and all controlled followers are disabled, the Q_{SB} control-logic signal goes high. The potential at the lower node of C_1 goes from 0V to $V_{C2}(t_S)=V_{INA}(t_S)$ because of the enabled B_3 follower. $V_{C2}(t_S)$ is the value of voltage stored on the C_2 capacitor before the transition of the $\overline{Q}_D$ signal to an inactive-low level. The potential at the upper node of C_1 consequently rises to the value of $V_{C2}(t_S)+V_{C1}(t_S)=V_{INA}(t_S)+V_{INB}(t_S)$, as the bottom waveform in **Figure 2** shows. This trace is the only analog waveform in this **figure**. The active-low-to-high transition of the sampling-command logic signal, Q_S, gets slightly delayed with respect to that of the Q_{SB} logic signal, suppressing glitches in the output voltage. When Q_S is high, the sampled voltage of $V_{INA}(t_S)+V_{INB}(t_S)$, which is present at Pin 7 of IC_2, passes through the enabled B_2 follower to the C_3 capacitor and gets stored there until the next sampling command. The A_3 follower serves as an impedance converter. Dual op amp IC_6 serves as a tapped delay line, which, in conjunction with one single-NOR gate and one dual-AND gate, derives properly timed internal logic-control signals from the single external logic-control signal, Q. EDN

REFERENCE

1 "AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ±250 mA Output Current and a Power-Saving Shutdown Mode," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.