



BY BONNIE BAKER



# Delta-sigma ADCs in a nutshell, part 3: the digital/decimator filter

Following the modulator in the delta-sigma ADC is a digital/decimator circuit. This circuit samples and filters the modulator stream of 1-bit codes. At the modulator output, high-frequency noise and high-speed sample rates are problems. However, because the signal now resides in the digital domain, you can apply a digital-filter function to attenuate the noise and a decimator function to slow the output data rate. Designers often intertwine the digital filter and decimator functions in the same silicon.

Figure 1 shows the signal as it travels through the digital/decimator-filter functions. The digital-filter function operates at the same rate as the modulator sampling rate (Figure 1a). Notice that the 24-bit code-train resembles the original signal (references 1 and 2). In the time domain, it looks like the digital-filter function is responsible for the low noise and high resolution of the delta-sigma converter. However, this function provides a second-order impact on the system noise by rejecting higher frequency noise, where the noise shaping from the modulator dominates noise reduction in the lower frequency band (Figure 1b).

The digital-filter function provides a digital version of the input, but the data rate is still too fast to be useful. Although it might appear that you have an abundance of high-quality, multibit samples at a high sampling rate, you don't need most of this data.

The second function of the digital/decimator filter is the decimator. Decimation is the process of reducing a digital signal's output rate to the system's Nyquist frequency. One simple way to implement a decimating function is to average together groups of 24-bit codes (Figure 1c). The decimator accumulates these high-resolution data words, averages several words together, outputs the average results,

and dumps the data for the next average. A more economical way to implement a low-power decimator function is to simply pick out a 24-bit word every Kth sample without performing additional averaging. (K is equal to the oversampling or decimation ratio.)

Almost all delta-sigma converters incorporate a class of averaging filters called sinc or FIR filters, named for their frequency response. Many delta-sigma devices use other filters with sinc filters for two-stage decimation. Low-speed industrial delta-sigma ADCs usually use only a sinc filter.

In the frequency domain, you can see that this digital/decimator filter simply applies a lowpass filter to the signal (Figure 1b). In so doing, the digital/decimator filter has attenuated the higher frequency-modulator quantization noise. With the reduced quantization noise, the signal re-emerges in the time domain.EDN

## REFERENCES

- 1 Baker, Bonnie, "Delta-sigma ADCs in a nutshell," *EDN*, Dec 14, 2007, pg 22, [www.edn.com/article/CA6512148](http://www.edn.com/article/CA6512148).
- 2 Baker, Bonnie, "Delta-sigma ADCs in a nutshell, part 2: the modulator," *EDN*, Jan 24, 2008, pg 24, [www.edn.com/article/CA6518678](http://www.edn.com/article/CA6518678).
- 3 Baker, R Jacob, *CMOS Mixed-Signal Circuit Design*, J Wiley & Sons, ISBN 0471227544.

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at [bonnie@ti.com](mailto:bonnie@ti.com).

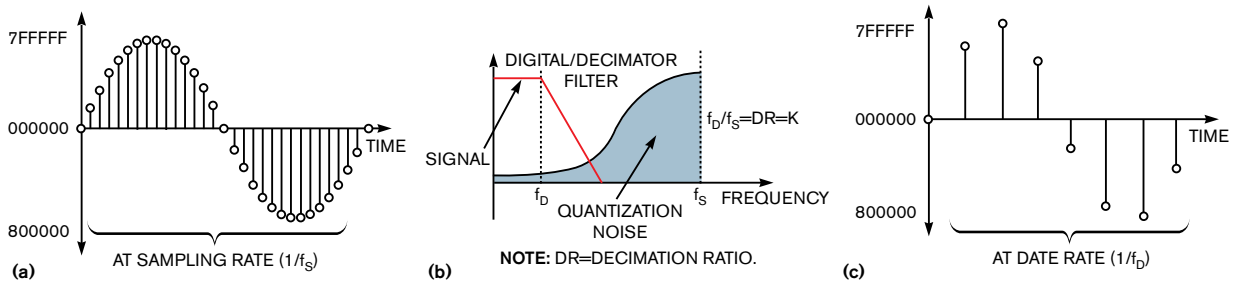


Figure 1 The digital-filter output function produces a high-resolution result (a), while rejecting high-frequency noise (b). The decimator function slows the output data rate (c).