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Delta-sigma ADCs in a nutshell, part 4: noise versus data rate

This article is the last in a brief overview of the inner workings of delta-sigma ADCs. You have seen how the modulator operates in the time and the frequency domains and how it shapes the conversion-quantization noise into higher frequencies. The modulator implements an oversampling system that has an integrator and negative feedback. You've also read about the inner workings of the digital/decimator filter. This filter

reduces the high-frequency noise in the digital 1-bit stream from the modulator while passing the digitized input signal to the converter output at a reduced data rate. The combination of these two modules yields a high-resolution ADC (references 1, 2, and 3).

With any converter, the actual resolution is equal to the number of bits the ADC transmits. "Effective resolution" describes the useful bits from an analog-to-digital conversion as they relate to signal noise. Effective resolution is equivalent to the ADC's effective number of bits. The ratio of the modulator's F_s (sampling rate) and F_D (output-data rate) define the decimation, or oversampling, ratio, which directly impacts effective resolution. The decimation ratio, whose value ranges from four to 32,768, equals the number of modulator samples per data output.

Consider the frequency spectrum in Figure 1. Suppose that you make the output data rate a small fraction of the modulator's sampling frequency (Figure 1a). The input frequencies from zero to F_D are in the output-signal band. The effective resolution is high because the noise level is low. A higher frequency for F_D increases the convert-

er's output-data rate and decreases the effective resolution. Most of the noise from the modulator is in the higher frequencies, but you still have a lower effective resolution (Figure 1b). Figure 1c shows an example of the relationship between decimation ratio and effective resolution of a sampling ADC.

One way to increase the output-data-rate speed without changing the effective resolution is to increase the modulator-sampling rate. You can increase this rate by increasing the master clock rate to the delta-sigma ADC. With a constant decimation ratio, both the sampling rate and the power consumption increase. Also, most converters have a practical limit for the sampling rate, beyond which they do not function properly. A strong relationship exists between the decimation ratio and effective resolution. Keeping the sample rate constant and lower data rates gives you high effective resolution at the output of the converter (references 4 and 5).EDN

REFERENCES

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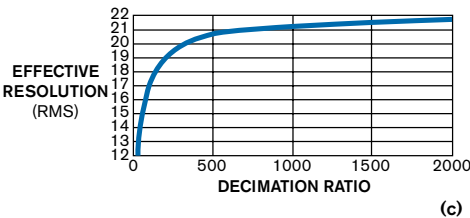
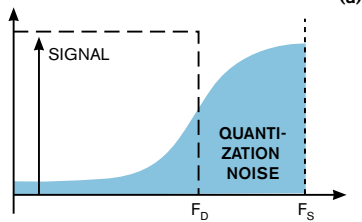
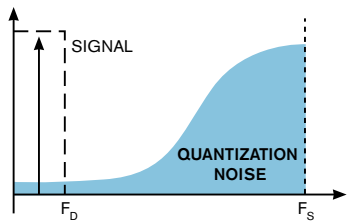


Figure 1 Decreasing the output data rate (a) or increasing the decimation ratio (b) produces a conversion with a higher effective resolution (c).