

Chop the noise gain to measure an op amp's real-time offset voltage

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One of the most important specifications of an op amp is its input-offset voltage. You can null out this voltage on many op amps, but the problem with determining the input-offset voltage is that the offset voltage varies with temperature, flicker noise, and long-term drift. Chopping and autozeroing techniques have been around for several years, reducing achievable input offset to microvolts or less. The accuracy is so good that other minuscule effects, such as copper-solder thermocouple junctions, dominate the errors, until, with some effort, you can overcome them, as well. This Design Idea introduces a new type of chopping. "Chopping the noise gain" is a simple way to measure the offset voltage in real time, so that you can subtract it and enhance dc precision.

Figure 1 shows an LTC6240HV op

amp in an inverting gain-of-10 configuration, along with several of its pertinent specifications. All of the input offset arrives at the output with a gain of 11 (called the "noise gain") as an output error. Any downstream circuitry or observer looking at the output voltage cannot distinguish the output error from the desired output signal.

Figure 2 shows the chop-the-noise-gain method. S_1 switches the additional shunt resistor, R_3 , in and out, changing the noise gain without affecting the signal gain or bandwidth. There would normally be some degradation of bandwidth, but C_1 dominates the bandwidth limitation whether the switch is open or closed. Now, you impose a small square wave on the output with an amplitude that is equal to the present dc errors. You can demodulate out the error as with a conventional chop-

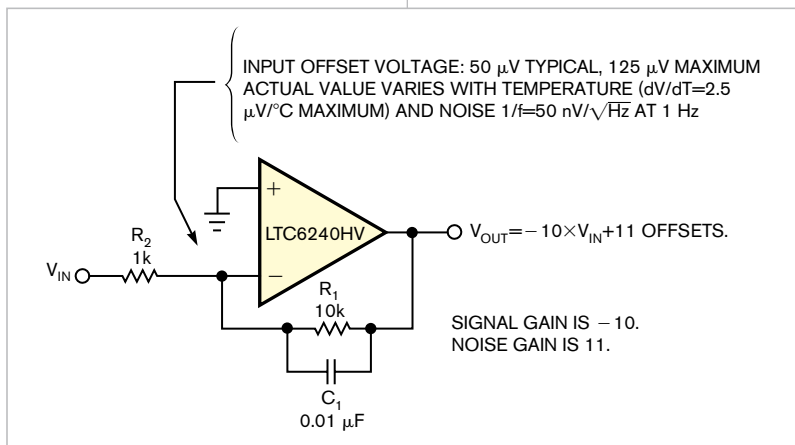


Figure 1 An op amp has a conventional gain of -10 . The noise gain is 11, so all of the input errors appear at the output with a gain of 11. You cannot distinguish the signal from noise just by looking at the output.

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per, or you can subtract it in software in a modern ADC-based system.

The circuit in Figure 2 is much like a simple summing amplifier, with one input both connected and disconnected. It is, in that sense, much like a true chopper amplifier. But, in this case, the input voltage being chopped is the amplifier offset, rather than the input signal. Why disconnect your input signal if you don't have to? Also, there is no need for continuous chopping; you need apply it only when you require an offset measurement.

Note that, although this Design Idea shows the inverting case for ease of understanding, the noninverting case is also practicable with a good analog switch for S_1 . Also, as with any sampled system, frequencies at or greater than the clock rate alias into baseband, and you should therefore filter them out before the chopping. Finally, this method does not correct for bias- or leakage-current-induced errors.

Switch S_1 opens and closes, increasing the noise gain and imposing the input errors onto the output with alternating noise gains of 11 and 22. The

resultant square wave now represents an easily measurable “11 errors,” which you can then subtract from the output. This technique is similar to that of conventional chopper amplifiers, except that, in this case, you are chopping the error rather than the signal.

Figure 3 shows the oscillogram of the output of the circuit of Figure 2, with an input voltage of 0V (grounded). The top trace is “S,” the control signal applied to S_1 at 750 Hz. The bottom trace is the output error alternating between 1 and 2 mV, indicating 90 μ V of op-amp offset. The output “sees” the effect of doubling the noise gain of the output offset. The difference between the two noise gains is 11, and this difference dictates the amplitude of the square wave that S_1 causes, independently of the input voltage.

Figure 4 is similar to Figure 3, but zoomed out and with a 2-mV-p-p slow-moving sine wave signal at the input

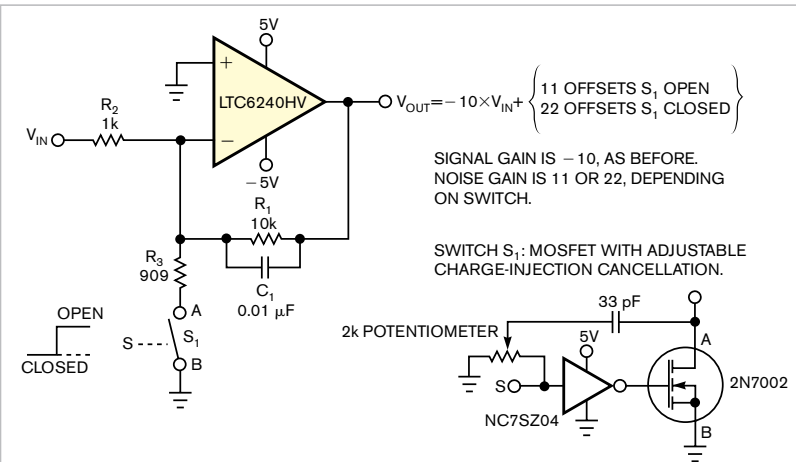


Figure 2 S_1 switches the additional shunt resistor, R_3 , in and out, changing the noise gain without affecting the signal gain or bandwidth.

voltage—that is, 20-mV-p-p output. The 1-mV square wave of Figure 3 is superimposed upon the slow-moving output signal and still contains the

real-time dc-error information. Just by looking at the output, you can discern that the true value of the signal is 1 mV below the measured value. **EDN**

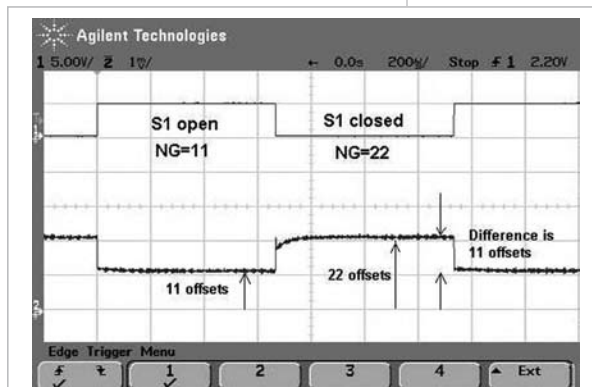


Figure 3 This oscillogram shows the output of the circuit in Figure 2, with an input voltage of 0V (grounded). The top trace is “S,” the control signal applied to S_1 at 750 Hz. The bottom trace is the output error alternating between 1 and 2 mV.

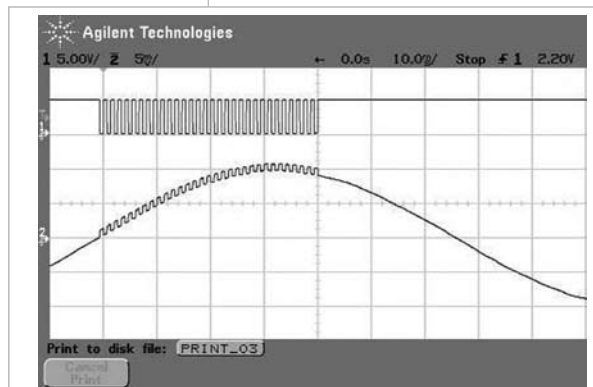


Figure 4 The oscillogram is similar to that in Figure 3, but with a 2-mV-p-p slow-moving sine wave signal applied at the input voltage.

Simple analog circuit provides voltage clipping and dc shifting for flash ADC

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Many flash ADCs, such as National Semiconductor’s (www.national.com) ADC1175, have a recommended operating input-voltage range of 0.6 to 2.6V (Reference 1).

However, in some applications, you must convert a symmetrical analog-input signal. The circuit in this Design Idea converts a symmetrical input-voltage range of -0.2 to +0.2V into

the recommended 0.6 to 2.6V range (Figure 1). The circuit also prevents the output voltage from going below -0.3V, which would probably damage the ADC.

The circuit uses an Analog Devices (www.analog.com) AD8002 dual-current-feedback operational amplifier to obtain a high bandwidth (Reference 2). The first block, noninverting am-

plifier IC_{1A} has a voltage gain of five. This block also provides high input impedance and low output impedance, so that the second block, IC_{1B}, operates properly. The second block does most of the work. Starting from a basic inverting amplifier comprising IC_{1B}, R₄, and R₅, you obtain the clipping effect by adding R₃ and D₁. R₃, D₁, R₄, and R₅ determine the clipping level. In addition, adding the I_{DC} current dc-shifts the output voltage. You can trim adjustable potentiometer resistor P₁ to obtain the desired output voltage shift—that is, 1.6V.

If diode D₁'s current is negligible, the output voltage, V_O, is $-(1+R_2/R_1) \times (R_5/(R_3+R_4)) \times V_1 + V_{CC} \times R_5/(R_6+P_1+R_7) = 1.6 - 5 \times V_1$. Given that the diode voltage, V_{DIODE}, is 0.6V_S, $V_O = -(R_5/R_4) \times V_{DIODE} + V_{CC} \times R_5/(R_6+P_1+R_7) = 1.6 - 1.65 = -0.05V$.

The clipping takes place near 0V, protecting the ADC. Raising the clipping level makes the circuit less linear in the nonclipping range. In other words, a design trade-off exists between clipping level and linearity. Resistor R₈ limits the current through the ADC's input pin. Capacitor C₂ is optional; it

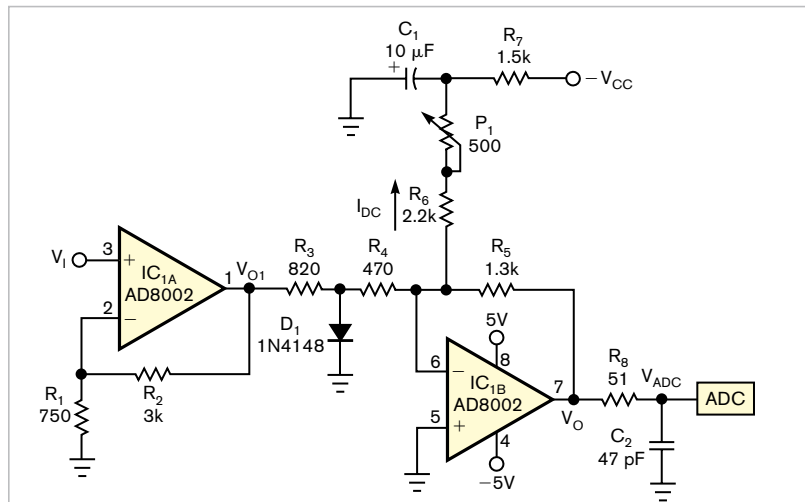


Figure 1 Adding R₃ and D₁ to a conventional op-amp circuit provides clipping. R₃, D₁, R₄, and R₅ determine the clipping level. In addition, adding the IDC current causes dc-shifting of the output voltage.

limits the V_{ADC}/V₁ bandwidth. Capacitor C₁ helps to reduce the voltage noise that might come from the -V_{CC} power supply. EDN

REFERENCES

- 1 "ADC1175 - 8-Bit, 20MHz, 60mW A/D Converter," National Semicon-

ductor, www.national.com/mpf/DC/ADC1175.html

- 2 "AD8002 Dual 600 MHz, 50 mW Current Feedback Amplifier," Analog Devices, www.analog.com/en/prod/0%2C2877%2CAD8002%2C00.html.

Compact laser-diode driver provides protection for precision-instrument use

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Continuous-wave laser diodes in precision-instrument applications require constant-current sources to drive them. Proper design of such a driver must involve careful tackling of robustness, stability, noise, and other issues and is consequently costly and complicated (Reference 1). Figure 1 shows a compact, cathode-grounded laser-diode driver with protection against ESD (electrostatic-discharge) damage, start-up spikes, overshoot, and possible fluctuation arising from external optical feedback. An op amp, IC₄, with an enable input drives PMOS FET Q₁ and controls the output current. R_S sets the current to the

rated value for a 35-mW HL6738MG laser diode from Opnext (www.opnext.com). To prevent output from Q₁ during start-up, comparator IC_{5A} keeps IC₄ off, and a 10-kΩ pullup resistor keeps Q₁ off by linking Q₁'s gate to the supply of IC₄ until the terminal supply, V_B, reaches the designed value, approximately 6.5V, and opens Q₁ via IC₄.

The key point for protection against ESD damage and overshoot lies in the use of Q₂, a depletion-mode NMOS FET. With power off, Q₂ conducts, shunting any harmful ESD to ground. With power on, comparator IC_{5B} outputs a negative voltage far below the gate-to-source off-state voltage. Hence,

Q₂ is off and has little effect upon the drive current unless the operating voltage at the laser's anode exceeds the maximum rating of 2.8V in the figure. In this case, the operating voltage triggers IC_{5B} to output high and thus turns on Q₂, shunting the drive current to ground, as well. The circuit now introduces significant hysteresis to latch off the state of emergency. Considering the low on-resistance of Q₂, this circuit provides better protection than the common method of relying on a paralleled zener diode for overshoot suppression (Reference 2).

Despite employing a split supply, this design requires no particular supply sequencing. You must cut off Q₂ only at the beginning of start-up, so it would be better to turn on the -9V external supply before enabling the driver. Despite the availability of substitutes for some ICs in this design, selection

sources in the figures) with resistors.

At the quiescent, 0V-input-voltage operating point, both halves of the circuit run at maximum current, and both the input and the output are at the same potential. When you impress a voltage on the input, you inject current into the Q_2 - Q_3 emitter node. From there, current can go up into base of Q_1 or down into base of Q_4 . The output voltage relative to the input voltage determines the direction of the injected current. If the input voltage is positive, it has no effect on the upper half because it is already limiting. It can, however, reduce drive current in the lower half, resulting in a reduction of lower output-drive current. Reduction of lower side output current results in a rise in output voltage. In short, an injected signal current “unlimits” the stage of opposite polarity.

At first glance, the circuit appears to have unity gain. But, because Q_2 and Q_3 sense the tops of R_2 and R_3

AN INJECTED SIGNAL CURRENT “UNLIMITS” THE STAGE OF OPPOSITE POLARITY.

and not circuit output, R_1 and R_2 are effectively in series with the output load. If the load's impedance, R_{LOAD} , is small, the circuit gets significantly loaded down. However, as long as the input stage does not clip, the circuit does not become distorted. The source driving the buffer stage sets $h_{FE}(Q_1) \times (R_1 + R_{LOAD}) \Omega$, where h_{FE} is forward-current gain.

Q_2 and Q_3 are common-base stages. Their purpose is to translate input voltage to the bias voltage that Q_1 and Q_4 require. This voltage-translation action allows direct substitution of other devices, such as MOSFETs or Darlington transistors. **EDN**

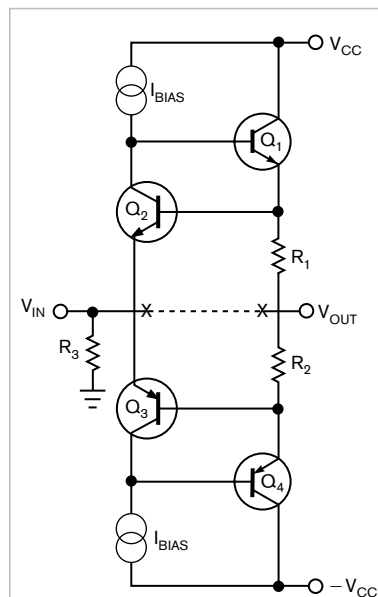


Figure 2 Adding another stage to the current source allows the circuit to function as a buffer.