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Use thermoelectric coolers with real-world heat sinks

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 Peltier devices, also known as solid-state refrigerators, or TECs (thermoelectric coolers), actively cool temperature-sensitive electronic components, such as optical detectors and

solid-state lasers. A glance at any TEC data sheet reveals that some primary and fairly easily understood parameters characterize a TEC: The maximum current is the TEC's current drive for

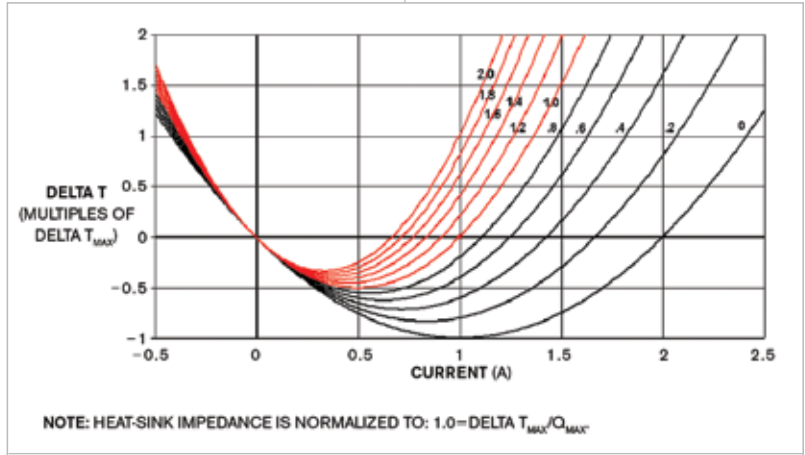


Figure 1 This family of curves shows that a thermoelectric cooler may actually heat rather than cool at the maximum drive current if the heat sink the cooler is mounted on is less than perfect.

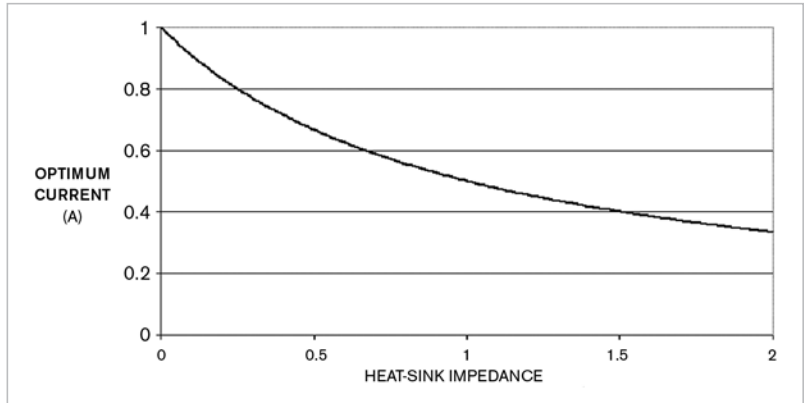



Figure 2 A derating factor for maximum voltage and current is based on the real-world thermal impedance of the TEC's heat sink.

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maximum cooling, the maximum differential temperature is the no-load cooling temperature at maximum current and with no heat load. The maximum voltage is the TEC's voltage drop at the maximum-current drive, and the maximum heat transfer (Q_{MAX}) is the maximum cooling-heat load at a maximum current and differential temperature of zero.

However, one TEC data sheet proviso that designers sometimes miss is that you always measure these parameters with the TEC mounted on an effectively zero-thermal-impedance—that is, perfect—heat sink. This point is an important one and deserving of the designer's rapt attention because heat sinks always have at least some thermal impedance, and all the primary TEC parameters change—sometimes dramatically—when the TEC must make do with an imperfect sink.

The family of impedance-versus-current curves in **Figure 1** illustrates this effect. Each curve corresponds to a different heat-sink thermal impedance, normalized to one for 11 values from zero to two.

Although the maximum current is, by definition, the optimal current for


maximum cooling at a heat-sink impedance of zero, the situation changes radically with increasing impedance until there's no net cooling whatsoever. Further, for impedance greater than

one, instead of cooling, the maximum TEC drive actually heats rather than cools. **Figure 2** shows the simple solution for this problem: You must replace the data sheet's maximum current and

voltage values with new, lower maximum-drive values corresponding to the optimal numbers you need to achieve maximum cooling whenever impedance is greater than zero. **EDN**

Interface MIDI instruments to a PC through a USB port

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 This Design Idea uses the FT-232BM from Future Technology Devices International (www.ftdichip.com), a USB-to-UART interface IC that you need not program, to interface a USB port to the MIDI (musical-instrument-digital-interface) bus (**Figure 1**). The USB signals directly interface to IC₁, an FT232BM. The serial-transmitter and -receiver signals pass through IC₂ and IC₃ to transform the RS-232 signals to the MIDI's loop current. You can use an EEPROM, IC₄, if you want to add a serial-number interface or use more than one interface.

This hardware doesn't require you to write any software. However, you must install two drivers. First, you need the free VCP driver from FTDI at www.ftdichip.com/Drivers/VCP.htm. It allows you to use this interface as a common serial-port interface. Before you install it, you must change a string in the file FTDIPORT.INF (**Reference 1**) to set up the 31,250-baud rate for FT232BM. Then, you can configure VCP to run at 38,400 baud. (The real baud rate will be 31,250 as preset in FTDIPORT.INI.)

Then, you must install another driver that permits you to see your VCP se-

rial port as a MIDI port for addressing all MIDI messages. You can find a lot of similar drivers on the Internet. For example, the Roland serial MIDI driver is available at: http://www.roland.it/download_drivers/for_win/serial32_wxp2k.exe. You can enable this driver on the COM1 or the COM3 port.

Listing 1, at www.edn.com/080417di1, shows the changes to add to the FTDIPORT.INF file that change the baud rate from 38,400 to 31,250 baud. Change this file before installation. **EDN**

REFERENCE

- 1 "FT232BM Designers Guide, Version 2," FTDI, 2002/2003, www.ftdichip.com/Documents/AppNotes/DF232_20.pdf.

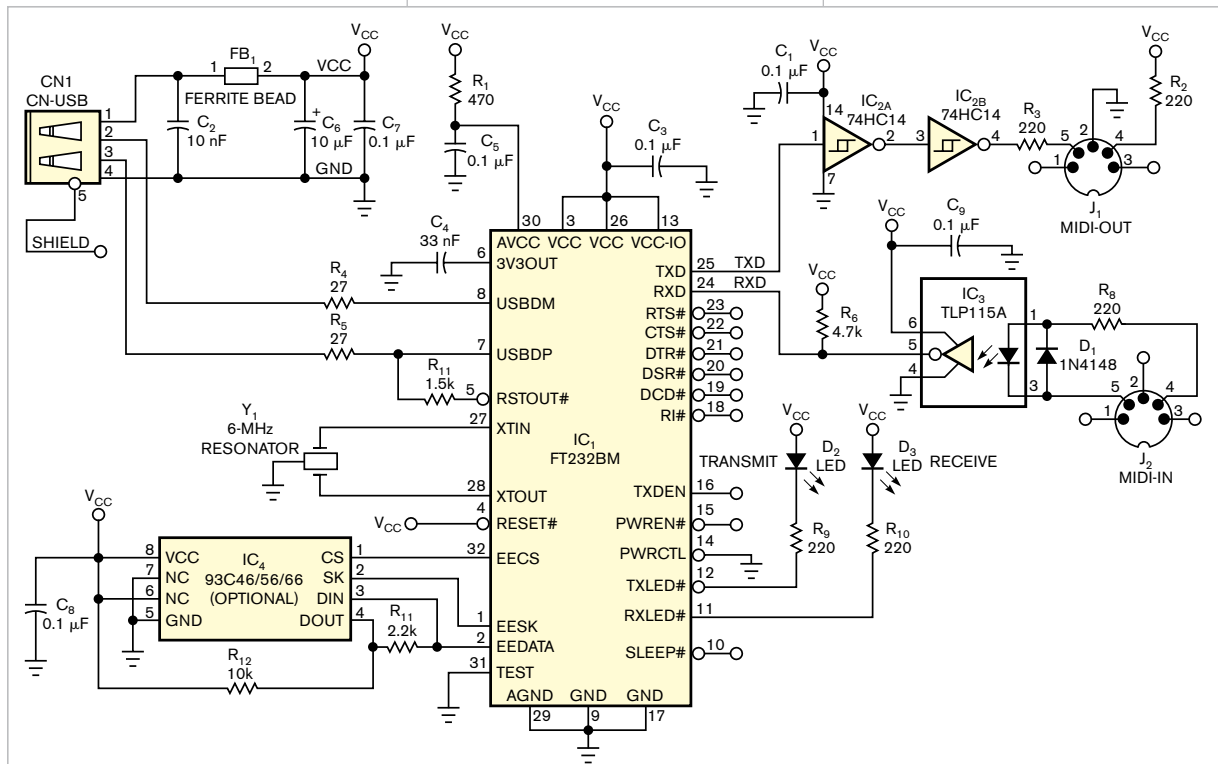


Figure 1 This USB-to-MIDI interface uses the FT232BM, a USB-to-UART interface chip that you need not program.

Transmission lines simulate digital filters in PSpice

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Designers use PSpice mainly to simulate analog circuits. However, you can also simulate digital filters with it. The main components in a digital filter are delay elements, adders, and multipliers. Although you can implement adders and multipliers using operational amplifiers, you can simulate a delay element with a transmission line. The transmission line in PSpice is a long-forgotten element that can realize a delay of seconds.

For example, **Figure 1** shows a second-order recursive digital filter. The transfer function for this filter is:

$$H(z) = \frac{B_0z^2 + B_1z + B_2}{z^2 + A_1z + A_2}$$

where $H(z)$ is the digital-filter-transfer function, z is the z -transform variable, the A s are the coefficients of the denominator polynomial of the transfer function, and the B s are the coefficients of the numerator polynomial of the transfer function. You can obtain the coefficient values with software avail-

able for filter design (**Reference 1**). The sampling frequency, f_s , relates to

the transmission-line delay as $t=1/f_s$. For example, a bandpass digital filter with a 3-dB passband from 900 Hz to 1 kHz, a sampling frequency of 6 kHz, and a Butterworth characteristic yields the following transfer function:

$$H(z) = \frac{z^2 - 1}{z^2 - 0.9096707z + 0.809374}$$

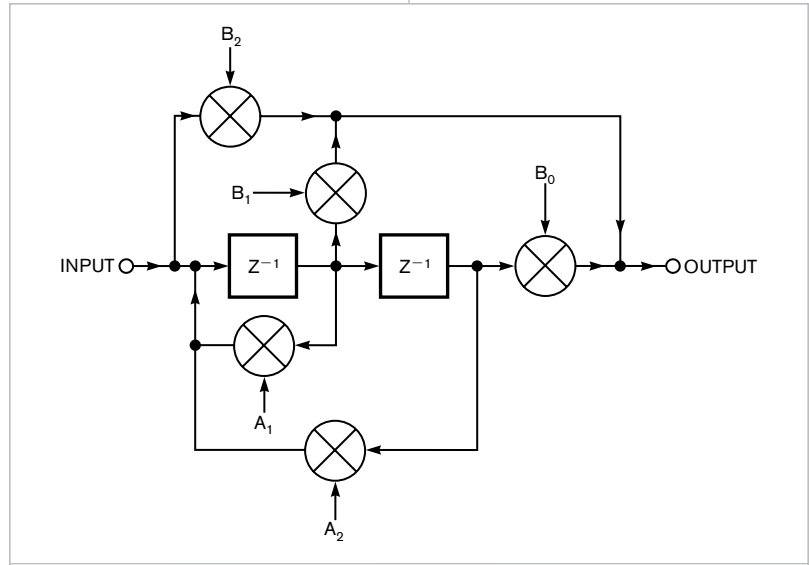


Figure 1 The transfer function for a second-order recursive digital filter has coefficient values that yield a lowpass, highpass, band-reject, or bandpass-transfer function.

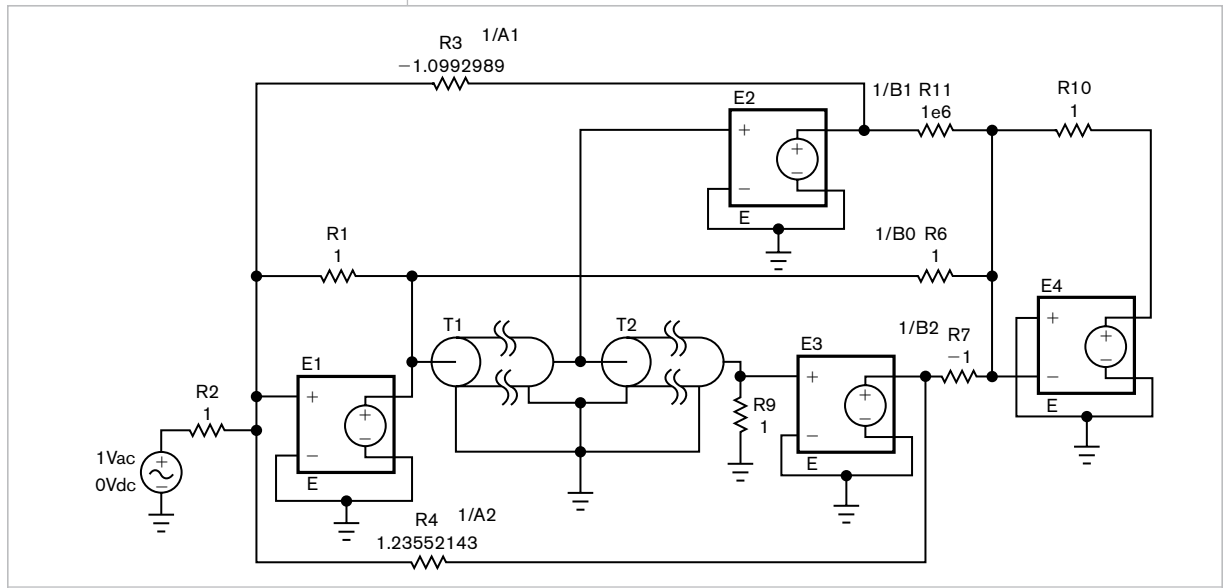


Figure 2 In the PSpice circuit, the VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers.

In this case, the transmission-line delay is $1/6000 = 166.67 \mu\text{sec}$. If you additionally specify an impedance, Z , of 1Ω for the transmission line, then the parameters for the transmission line are $Z_0 = 1\Omega$, and $t = 166.67 \mu\text{sec}$. **Figure 2** shows the PSpice circuit. The VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers. **Figure 3** shows the results of the simulation. **EDN**

REFERENCE

■ López, David Báez, "Windows Based Filter Design with Winfilters," *IEEE Circuits and Devices*, Volume 13, 1997, pg 3.

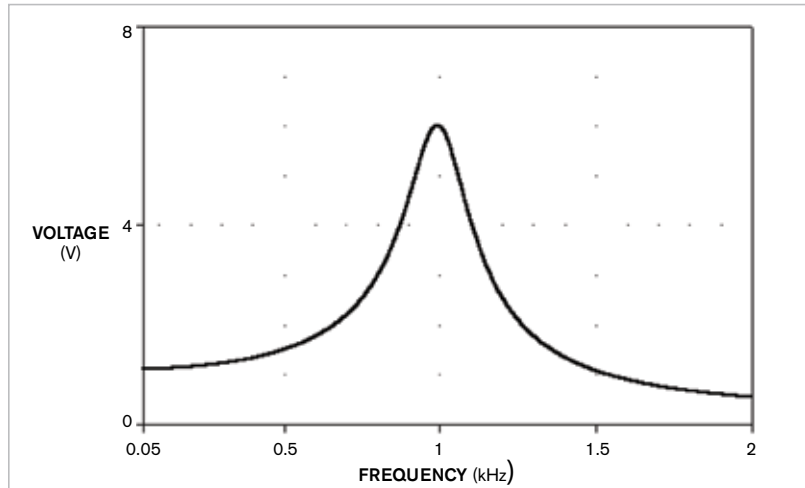


Figure 3 In this PSpice simulation, the digital bandpass filter uses transmission lines as delay lines.

Dual flip-flop forms simple delayed-pulse generator

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Some applications require clock-timing adjustments, such as generating precision clocks for time-interleaved ADCs, or delay adjustments in a variety of precision-tim-

ing and pulse-delay applications. This Design Idea describes a delayed-pulse generator using a dual-CMOS D-type flip-flop (**Figure 1**). The circuit provides precision time delays of a trigger-

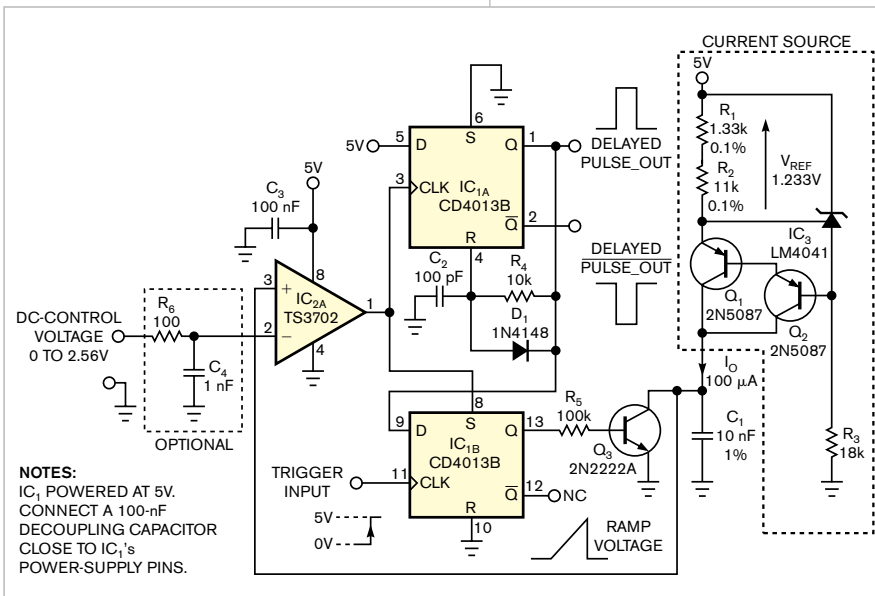


Figure 1 The rising edge of a trigger input starts a precision ramp voltage that compares with a control voltage, generating a precise delay.

input pulse. A dc-control voltage selects a time delay within the full-scale range. When the rising edge of a pulse triggers the input, the circuit's output generates a pulse with its rising edge delayed by an amount equal to the selected time delay, T_{PD} , plus a fixed inherent propagation delay T_{PD} . Also, a time constant, R_4C_2 , determines the output pulse's width.

A precision dc source, I_O , and capacitor C_1 set the full-scale delay range. When Q_3 is off, the current source charges capacitor C_1 , generating a linear-ramp voltage with slope equal to I_O/C_1 . The delay is the time it takes for the ramp to rise from its initial voltage to the control-voltage value.

In this application, the ramp slope is $10 \text{ mV}/1 \mu\text{sec}$, so that the full-scale delay range is $256 \mu\text{sec}$ for a control voltage of 0 to 2.56V. You can set the full-scale delay by changing I_O through either $R_1 + R_2$ or capacitor C_1 . For best accuracy, the current source can range from $10 \mu\text{A}$ to 1 mA, the capacitor's value can range from 1 nF to $1 \mu\text{F}$, and the corresponding full-scale delay can range from $2.56 \mu\text{sec}$ to 256 msec. Use a precision film capacitor for C_1 .

The basis of the current source is a shunt precision-micropower-voltage-reference, IC_3 , producing a reference voltage of 1.233V with an initial ac-

curacy of 0.2%. A Texas Instruments (www.ti.com) LM4041, through precision resistors R_1 and R_2 , biases the Darlington-coupled transistors Q_1 and Q_2 with a reference current $I_O = V_{REF} / (R_1 + R_2) = 100 \mu A$. The Darlington configuration ensures that base current is negligible and that the output collector current can achieve a worst-case accuracy of 0.3%. You can use any small-signal transistor, but, for best accuracy, use high-gain, low-level, low-noise BJTs, (bipolar-junction transistors) such as a 2N5087 or a BC557C.

IC_{1A} is a one-shot circuit (**Reference 1**). The output pulse's width, T_w , is $R_4 C_2 \times \ln(V_{DD} / V_{TH})$, where V_{TH} is the threshold voltage of the digital CMOS. Because $V_{TH} \approx V_{DD} / 2$, then $T_w \approx R_4 C_2 \times 0.69$. Diode D_1 reduces recovery time. After power-up, Q_3 is in saturation, absorbing the current source's output, and, as soon as an input pulse triggers the circuit, IC_{1B} 's Q output goes low, switching off Q_3 , starting a ramp. When the ramp exceeds the control voltage, then the IC_{2A} compar-

ator's output goes high, and the rising edge triggers one-shot IC_{1A} , and switches on Q_3 through IC_{1B} , allowing the discharge of the capacitor C_1 . When an input pulse triggers the circuit, any other trigger pulse that occurs before the falling edge of the delayed output pulse does not produce an output pulse; in other words, the circuit is not retrig-gerable. This feature permits you, at the same time, to divide and delay an input-trigger clock.

Although IC_1 and IC_2 can operate from a 3 to 16V supply, the minimum supply voltage of the circuit is 5V; otherwise, Q_1 and Q_2 approach saturation, generating to a less linear ramp voltage. Voltage comparator IC_{2A} , an STMicroelectronics (www.st.com) TS3702, has an input-common-mode-voltage range that includes ground, permitting you to monitor input voltages as low as 0V.

However, for correct operation of the circuit, the minimum control voltage must be greater than the saturation voltage of Q_3 . For the components in

Figure 1, the measured value is 12 mV. If you want to reduce this voltage, you can use a digital N-channel MOSFET with low on-resistance. The optional input lowpass filter, comprising R_6 and C_4 , helps to clean noise from the dc-control voltage.

If a DAC drives the control input, you can build a digitally programmable delay generator. A suitable low-cost, 8-bit DAC is the AD558 from Analog Devices (www.analog.com), which features an internal precision bandgap reference to provide an output voltage of 0 to 2.56V, making 1 LSB equal to 1 μ sec. It operates from 5 to 16V, with a 1- μ sec settling time. The circuit's quiescent current, I_{DD} , is less than 300 μA because all ICs are micropower. **EDN**

REFERENCE

■ Bhandarkar, Santosh, "Single-IC-based electronic circuit replaces mechanical switch" *EDN*, March 15, 2007, pg 76, www.edn.com/article/CA6421439.