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## Third-party-IP providers: physical-design questions, part one

**A**s this column has discussed previously, selecting an IP (intellectual-property) provider involves several technical and business issues. On the technical front, the additional levels of selection complexity involve the physical-design view of the IP. The issues that follow assume that the IP under consideration meets the design and performance specification and targets the correct process-technology option. In addition to your architectural and performance goals, six categories of the physical view should be part of the selection criteria for the IP: block pins and grid, blockages and overlayer routing, power supplies, global signals, placement and rotation, and embedded blocks and clocks.

You should have a good understanding of the first category—block pins and grid—as it's been around for more than 30 years. The most important aspect to understand is that a design will support multiple simultaneous grids that all relate to different functions and criteria during the design. All of these

grids should be related integral multiples of at least one of the other grids.

The minimum grid is the database resolution. Next come the mask-fracture/e-beam-spot-size resolution, the minimum drawn data (digitizing) grid, the routing grids, and the cell-placement grid; none of these values is the same as the minimum database-resolution grid value.

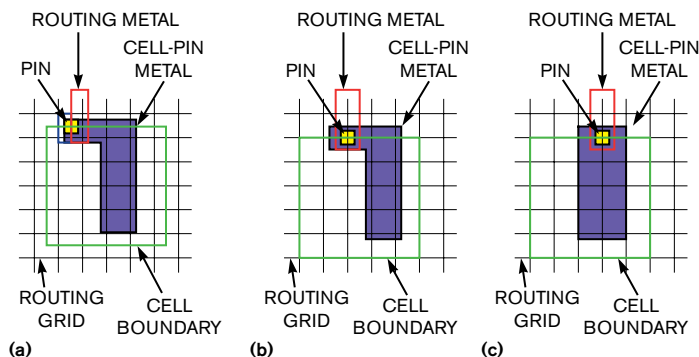
Process geometries that exceed one wavelength require only simple MDP (mask-data prep), DFM (design for manufacturing), and OPC (optical-

proximity correction). These options can support wire jogs that come from nonaligned or off-grid pins and wires. In these processes, connectivity is the main driver, and you can use standard subgrid routers, which simply allow DRC-clean wiring by shifting wires to the digitizing grids from the X- and Y-direction router-grid values.

In such simple cases, you can make off-grid pins and connections anywhere on the line without major consequences. In subwavelength processes, however, connections need to be clean, with no overhang and preferably all in the same direction. Otherwise, the DFM and OPC create context-specific options that are data-intensive and impact reliability. **Figure 1** depicts examples of these cases.

Select physical IP with the manufacturability of the block in mind. It is inappropriate to use IP created with both X and Y routing-grid pitches that differ from the pitches your SOC (system-on-chip) assembly uses. If the IP is incompatible with your flow, ask the provider to change the PHY (physical)-layer view so it aligns with your flow, change the technology files and grid structures of the place-and-route environment and for the whole SOC, or choose another IP-block/provider. Never modify the IP yourself; you can't be sure of the impact of your changes.

As for the pins themselves, there are several basic criteria that the plethora of new IP providers is leaving behind: Any part of the IP block that connects at a level of hierarchy above the block must have a pin; all pins in the layout should appear in the netlist views; all pins in the netlist should appear in the layout view; and the power-supply pins must have names that identify the correct operating-voltage rail. The last issue is a new pin-naming criterion that arose from the various power-reduction and multivoltage-operation techniques. **EDN**



**Figure 1** You can make off-grid pins and connections anywhere on the line without major consequences (a). In subwavelength processes, connections must be on-grid with no overhang (b and c).

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