

The megapixel race: a chip designer's point of view

AS CMOS IMAGE SENSORS HAVE MIGRATED FROM LOW-END APPLICATIONS TO MULTIMEGAPIXEL CAMERAS, EMPHASIS HAS SHIFTED FROM INTEGRATING DIGITAL CIRCUITS TO THE FUNDAMENTAL DESIGN OF THE PIXEL ITSELF.

During the operating, or integration, mode, visible photons generate electrons in the pixel cell of a CMOS image sensor. The pixel collects the electrons and then translates the accumulated charge to voltage signals that serve as an output. Expressing this process quantitatively, pixel responsivity is the relation between the electrical signal and its exposure to light ($V/\text{lux} \times \text{sec}$). “Full-well capacity” is the number of electrons that the pixel can collect. Dynamic range is roughly the number of resolvable gray levels, which you calculate by dividing the maximum signal by the minimum detectable signal and usually report in decibels.

Thermally generated electrons are obviously enemies of image sensors, because the pixel collects them along with optically generated electrons; they steal well capacity and add noise. Thus, the rate of the electrons’ thermal generation within the pixel, or “dark current,” is a major performance measurement that you generally report in electrons per second. Pixel development requires simultaneous optimization of all of the above parameters, along with a few additional ones—a major challenge within the world of pixel design.

Inside each pixel are a light-sensitive diode and at least three transistors. As resolution increases, transistors must be very small to allow as much area as possible where the diode can collect light. That necessity requires advanced CMOS processes. But in processes of 180 nm or less, transistors need strong well implants and shallow source-and-drain implants that cause higher junction leakage and eventually increase the dark current in the CMOS pixel array. Also, STI (shallow-trench isolation) between the transistors causes stress and increases the number of defects within the silicon, which again gives rise to higher dark current. To understand the complexity of this problem, explore the operation of a pixel and then look at optimizations.

OPERATING PRINCIPLES

Figure 1 shows a pixel with three transistors and a photo diode. A photon hits the silicon, generating an electron and a hole. This electron-hole pair travels together in the silicon until it encounters an electric field, in which the electron moves toward the higher voltage, and the hole migrates toward the ground. Within the CMOS pixel, a photo diode—usually

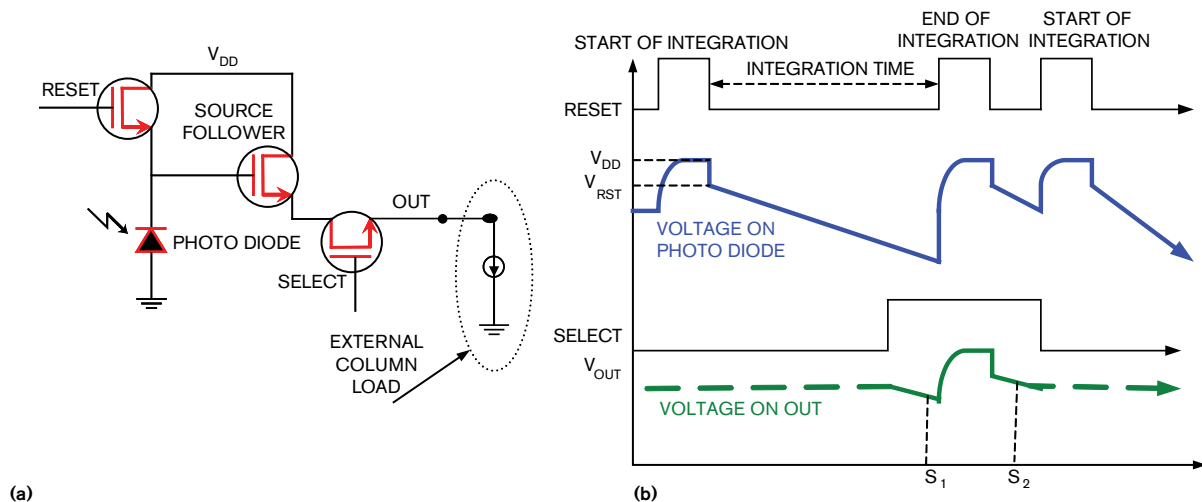


Figure 1 A typical CMOS pixel has three transistors and a photo diode (a). Typical “rolling-shutter” timing samples the signal twice (b).

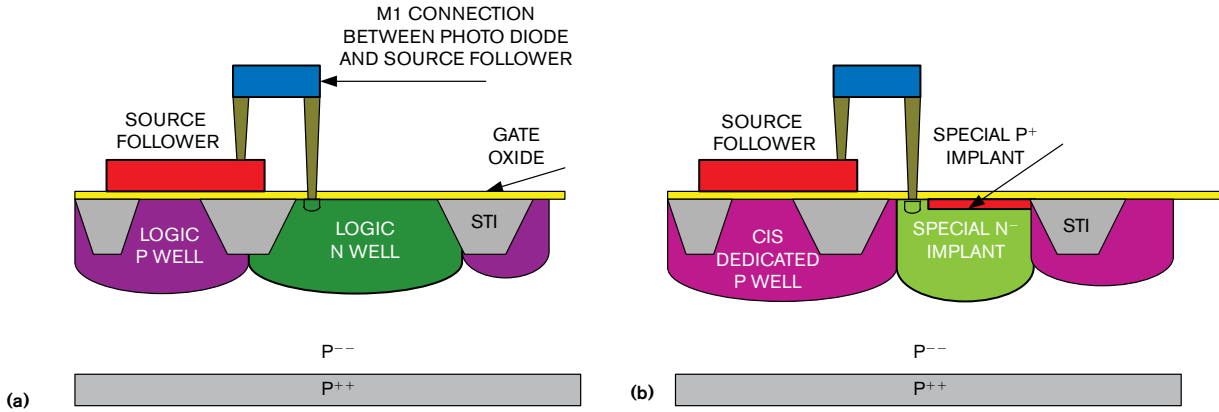


Figure 2 A cross-section of a typical CMOS-image-sensor front end adds no process steps on top of the plain-vanilla CMOS (a). A state-of-the-art CMOS-image-sensor front end adds three front-end-process steps (b).

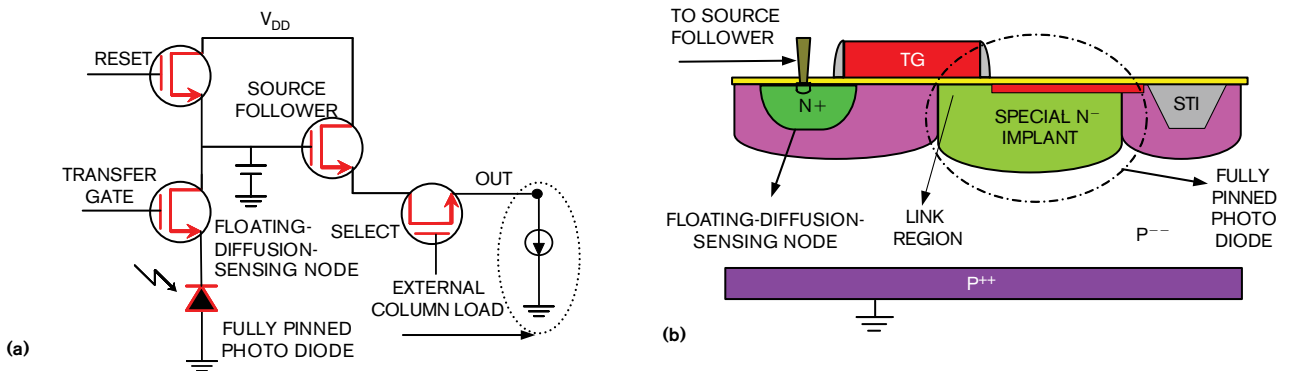
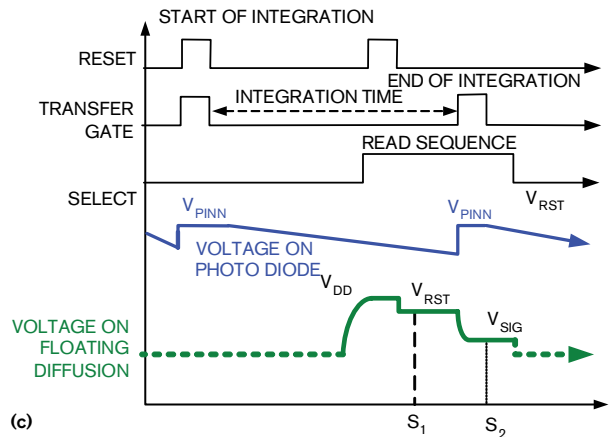


Figure 3 An electrical diagram of a four-transistor pixel has a fully pinned photo diode (a) that you can view in cross-section along with the transfer-gate transistor (b). In a typical timing diagram for a four-transistor pixel, the integration starts by activating the reset and transfer-gate transistors and setting the diode to its pinned potential (c).



an N-type implant in a P-type region—generates the separating electric field.

The photo electrons accumulate in the diode and cause a drop in voltage that is proportional to their number. The number of photo electrons is, in turn, proportional to the photon flux. Thus, the voltage drop in the diode is proportional to the photon flux. To increase this signal pixel, designers employ quantum efficiency—increasing the number of electrons for a given photon flux. They also try to increase the voltage drop on the diode for a given charge. This value is the “pixel-conversion gain,” and it is inversely proportional to the photo diode’s capacitance.

You optimize the quantum efficiency of a photo diode by engineering it so that its electric field penetrates deeply into the silicon. This step is important for photons in the green-to-red spectrum, because photons with longer wavelengths tend to penetrate deeper into the silicon. It helps to replace the standard starting material with low-doped, P-type epitaxial material grown on P⁺⁺ substrate.

In the first generation of the three-transistor pixel, design-

ers made the diode by implanting the regular PMOS N well into the P⁻ substrate (**Figure 2a**). Another common approach was to use the N⁺⁺ of the NMOS-transistor source-and-drain implant. Although these options are fully compatible with the regular CMOS process, the resulting diode exhibits poor performance. For example, using a large N-well diode, which you need for good collection of photo electrons, causes the pixel capacitance to be excessive. Thus, the overall efficiency of translating photon flux to voltage drops becomes lower than necessary.

Another serious problem with diodes that are based on CMOS implants is their typical dark current. Dark current af-

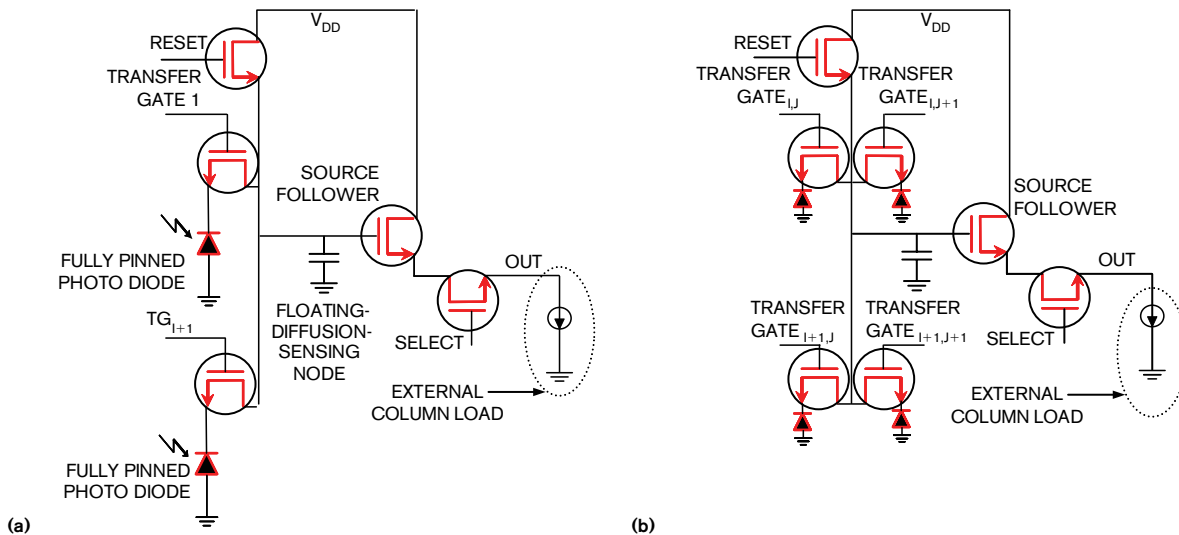


Figure 4 An electrical diagram of a two-shared configuration uses mature pinned-photo-diode technology, arranging the photo diodes and their associated transfer-gate rows. There is one reset, one select, and one source-follower transistor for each group of pixels in two consecutive rows (a). A four-shared configuration uses mature pinned-photo-diode technology, arranging the photo diodes and their associated transfer gates in a 2×2 configuration. There is one reset, one select, and one source-follower transistor for each group of pixels in two consecutive columns and rows (b).

ffects the noise floor of the pixel and thus determines the low level of illumination a pixel can integrate and still have meaningful data. For good image quality, it must be smaller than $100e/\text{sec}$ per pixel, where e is electrons. You can set much lower and more aggressive values than the in-room temperature to ensure that the dark current does not deteriorate the image quality—even at 60°C . The dark current depends on several factors: the diode temperature, the number of silicon defects near the diode’s electric field, and the electric-field strength.

Because regular CMOS implants are not optimized for low leakage, they usually exhibit a dark current of approximately $1000e/\text{sec}$ for the N-well implant (one order of magnitude higher than needed) and even higher for a source-and-drain implant. The situation is even worse, because the N^{++} implants induce defects in the surrounding silicon. The implant anneal typically cures these defects, but, when you try to manufacture several-megapixel arrays, some of the N^{++} diodes have significantly higher dark current than the average. Such pixels with excessive dark current appear in a black picture as twinkling or shining stars. Because our eyes are immediately drawn to high-frequency perturbation in the image, these leaky pixels ruin the overall image quality; if they cluster together, they make the entire chip unusable.

THE PIXEL TRANSISTORS

The role of the source-follower transistor in the pixel is to decouple the photo diode from all other pixels that connect to the same column-output line. When the row-select transistor is open, the column-current source maintains a few microamps in the source-follower transistor. In theory, the source-follower transistor will support this current as long as the voltage at its source is $V_S = G_{SF} \times V_{PD} - V_{TRSF}$ and $V_{PD} > V_{TRSF}$ where G_{SF} is the source-follower gain, V_{PD} is the photo-diode voltage, and V_{TRSF} is the source-follower threshold voltage. In

an ideal case, V_S is linear with V_{PD} . However, in a typical logic transistor V_{TRSF} increases with V_S , making the first equation highly nonlinear and reducing the dynamic range of the pixel. A common approach to this problem is to replace the P-well implants of the logic transistors with a carefully designed new P well that makes the source-follower transistor immune to this effect.

Figure 2 illustrates a first-generation three-transistor pixel with no additional masks, compared with a state-of-the-art pixel requiring three additional masks. You use the first mask for a special photo-diode N^- implant, which gives the exact capacitance for a given pixel design. The second mask is a P^+ mask that prevents electric fields from reaching the surface, significantly reducing the dark current. Notice that, because in a three-transistor design, you need to directly connect the photo diode and source-follower transistor, the P^+ implant does not cover a small region near the diode’s contact. This diode is partially buried. The P^+ implant also creates another separation field near the diode surface, which helps to increase the quantum efficiency for blue photons.

The third mask reduces the body effect of the source-follower transistor, making its threshold voltage immune to changes in source voltage. These changes apply only in the pixel array; the array periphery, including controls, ADCs, and DSP, still uses the well-established and optimized logic-CMOS process.

The main problem that makes the three-transistor pixel unusable for small pixels is that, as the number of photons available for collection decreases, the signal decreases. To maintain the same SNR (signal-to-noise ratio), you must suppress noise sources.

The main noise source in dark areas, once you suppress the dark current, is the so-called reset noise. Referring back to **Figure 1b**, you begin integration by setting the photo diode to high voltage by pulsing the reset transistor. When the re-

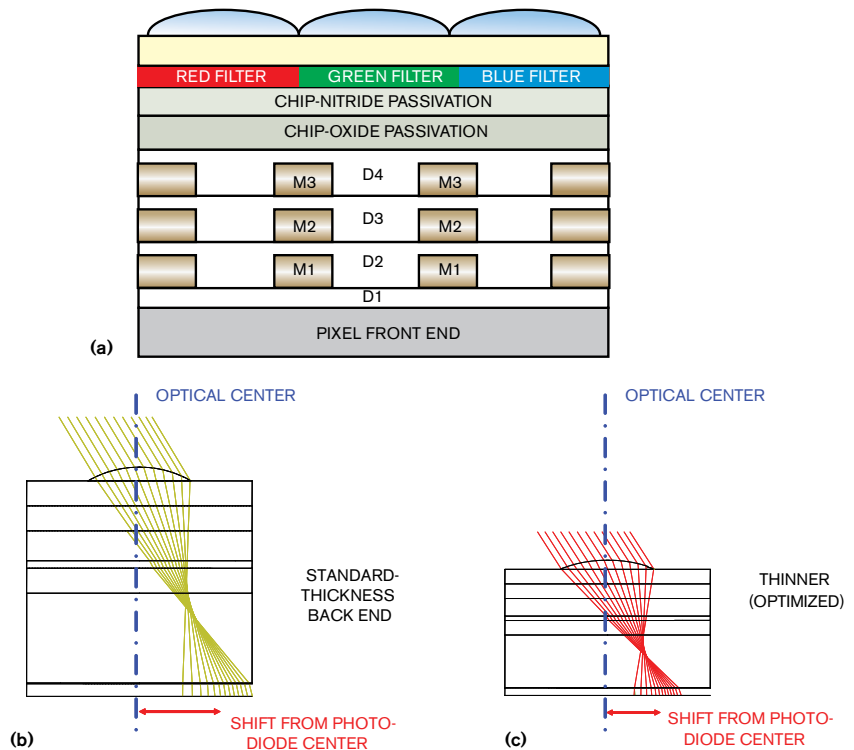


Figure 5 A typical CMOS image sensor uses three metal layers inside the pixel and four layers of metal in the periphery (a). The angle of incidence of light depends on the pixel's location in the array—whether for a standard CMOS back end (b) or an optimized CMOS-image-sensor back end (c).

set transistor returns to idle, the diode starts collecting photons, and its voltage decreases. At the end of the integration time (S_1), the output voltage copies to an analog memory in the column circuit. Again pulsing the reset gate sets the diode to high voltage, which copies to another analog memory (S_2) in the column amplifier.

The photon flux is theoretically proportional to the difference between these two voltages that the analog memory stores. But, because the start-of-integration-reset event and the read-reset event can't be simultaneous, the sample of diode high voltage that the system sends to the column amplifier is not exactly equal to the diode voltage at the beginning of integration, significantly contributing to noise. The common way to eliminate this noise is to use a four-transistor pixel and a fully pinned photo diode.

THE FOUR-TRANSISTOR PIXEL

Figure 3a shows a four-transistor CMOS-image-sensor pixel, including a fully pinned photo diode. The fully pinned diode has relatively small free-

charge capacity. The construction of the diode is similar to that of the partially buried photo diode in **Figure 2b** but with one significant change: There is no contact between the photo diode and source-follower transistor, virtually eliminating the surface contribution to dark current.

With a fully pinned and properly designed photo diode, all free electrons from the diode flow out when the reset and transfer-gate transistors are active. In that case, the potential in the diode reaches its minimum value—the pinned potential, which it reaches repeatedly every time you evacuate all electrons from the diode. This feature enables noise reduction and is the main advantage of the fully pinned photo diode over conventional diodes.

Figure 3c illustrates proper four-transistor-pixel operation. The integration starts by activating the reset and transfer-gate transistors and setting the diode to its pinned potential. After integration, the reset transistor activates and sets the floating-diffusion capacitor to high voltage and copies this voltage to the first

memory bank at the column circuit. Opening the transfer-gate transistor then transfers the photo electrons to the floating-diffusion capacitor. The resulting voltage of the capacitor then copies to the second memory bank at the column circuit. You calculate the photo signal by subtracting the signal voltage from the reset voltage. Although the reset voltage is noisy because its value fluctuates every time you reset the floating-diffusion capacitor, the photo signal itself is noise-free, as long as you get all electrons in the photo diode into the capacitor.

To ensure low-noise operation, this cycle must collect all the electrons from the diode through the link region between the diode and the transfer gate. This task is the main optimization duty for a four-transistor pixel. Pixel designers do this optimization by changing the layout and the implant. This scheme is not scalable in any way, and you have to start almost from scratch for each new pixel-size design.

Another optimization of a typical four-transistor design is the reduction in temporal noise of the source-follower transistor, which becomes dominant when you've eliminated other sources. The transistor noise is mainly due to defects in its gate oxide and on the shallow-trench-isolation interface with silicon. To reduce or eliminate these defects, you must open the most difficult process modules in a given CMOS-process node and reoptimize them. But, as pixels become smaller, this activity becomes inevitable to keep SNR constant.

FURTHER OPTIMIZATION

One way of retaining both a big diode and a big optical opening in a small pixel is to share several photo diodes and their associated transfer gates with one floating-diffusion capacitor, one reset transistor, one source-follower transistor, and one row-select transistor. **Figure 4a** shows a “two-shared” pixel. In this example, there are five transistors on two photo diodes, resulting in 2.5 transistors per diode, an even better ratio than that of the three-transistor pixel. This configuration is beneficial for pixels larger than 2.5 microns. For smaller pixels, a “four-shared” configuration with only 1.75 transistors per photo diode is common (**Figure 4b**). Although it seems attractive to increase the number of shared photo diodes and

hence to decrease the photo-insensitive area, there is a physical limit to doing so. The floating-diffusion capacitance tends to increase linearly with the number of shared transfer gates, causing a decrease in pixel responsiveness.

THE OPTICAL STACK

You know how to modify the pixel front end of an ordinary CMOS process to increase response and reduce pixel noise. In parallel, innovative efforts are under way to optimize the pixel's optical stack, thus improving the optical path to the silicon.

Figure 5a shows the typical back-end scheme of a CMOS image sensor. A typical CMOS image sensor uses three metal layers inside the pixel and four layers of metal in the periphery. The passivation layer typically comprises oxide and nitride and resides above the last interdielectric layer—D4 in the case of the four-level metal stacks. The red, green, and blue polymeric filters, which are responsible for the color reproduction of the images, reside above the passivation layer. (A single pixel without a color filter can provide only monochrome information.) The microlens that directs the light into the photodiode resides above the color filter.

The microlens must cover most of the pixel area to gather even the light that impinges on the periphery of the pixel. However, producing the microlenses with no space between them is difficult and usually results in some photo-response nonuniformity: the main noise source in medium to high illuminations. Second, you must determine the height of the microlens. Here, you choose a focus point between M1 and M2 of the pixel. Because the focus point is a function of microlens curvature, itself a function of pixel size, microlens space, and microlens height, pixel designers must repeat the optimization of the focus point for each reduction of pixel size.

The angle of incidence of light depends on the pixel's location in the array. The pixels near the edges of the array get most of their light at some angle to the optical axis, so the focus point for these pixels is not in the center of the pixel. The shift depends heavily on the height of the total stack between the microlens and the silicon surface (**Figure 5b**).

Two improvements can help. Designers can shift the optical axis of the mi-

crozens at the center of the photo diode within the middle of the array by the needed amount to direct angled rays to the diode's center. This operation is simple, but it requires good simulation tools and knowledge of the lens system of the final camera. Designers can also reduce the stack height by decreasing the metal and interdielectric thicknesses. This task is complicated and, by definition, changes major characteristics of the baseline-

CMOS process. It also requires additional qualification of the technology. The change is so far-reaching that some of the CMOS modules in the periphery require redesign.

Some CMOS-image-sensor companies have recently moved to copper back-end processes. For copper, the interdielectric layers comprise layers of oxide and nitride. Because this structure is built exactly like an interference filter, some of the visible

spectrum photons cannot reach the surface, making a copper CMOS back end unsuitable for image sensors. The main reason to move to a copper-back-end process is the availability of fine-lithography features with CMOS technology based on copper. To adapt this advanced fabrication technique to CMOS image sensors, a special process replaces the nitride layers in the interdielectric with oxide.

Bringing the light from the chip surface to the diode is one of the biggest unsolved tasks for pixels of less than 1 micron. Companies are trying to implement radical changes into their processes to design even smaller pixels. Consider the back-side-illumination scheme, which companies base on photons coming from the back side of the silicon—to the pixel—without encountering the pixel-metallization layers. A different yet novel approach is to use a wave-guiding scheme, which you base on the creation of miniature structures above each pixel to guide the light from the surface of the chip to the diode.

Achieving good CMOS-image-sensor performance is a complex task. However, scientists and engineers are trying new and inventive ideas that will no doubt produce clearer and crisper images using increasingly smaller pixels in megapixel-image-sensor arrays. **EDN**

AUTHORS' BIOGRAPHIES



Assaf Lahav is chief pixel designer for the CMOS-image-sensor R&D group at Tower Semiconductor, where he serves as lead engineer, developing advanced pixels, mainly for cellular-phone applications, and working on high-end imaging arrays. He holds bachelor's, master's, and doctorate degrees from Technion, Israel Institute of Technology (Haifa).



Amos Fenigstein holds bachelor's, master's, and doctorate degrees from Technion, Israel Institute of Technology (Haifa). He worked with SCD on the state-of-the-art MCT for infrared-image sensors until 1998. From 1998 to 2001, Fenigstein was with Intel, managing a failure-analysis team. Since 2001, he has been with Tower Semiconductor, serving as director of R&D for CMOS image sensors and the company's nonvolatile memory-product line.