Synopsys / ANTUN DOMIC

How DFT conquers GROWING CHIP COMPLEXITY

Synopsys' Antun Domic talks about the role of design for test in curbing costs and ensuring reliability.

JOINING SYNOPSYS IN 1997, Antun Domic, PhD, now manages the Implementation Group, which is responsible for the company's flagship synthesis and physical-design products, as well as test-automation, signal-integrity, power-analysis, and timing and formal-verification products. Before joining Synopsys, he worked at Cadence Design Systems, Digital Equipment Corp, and the Massachusetts Institute of Technology's Lincoln Laboratory. Domic holds a doctorate in mathematics from MIT and a bachelor's degree in mathematics and electrical engineering from the University of Chile.

Is DFT (design for test) strictly the domain of dedicated DFT engineers?

Certainly, there are DFT specialists, and their responsibility is to construct the DFT strategy for the chip. But verification engineers also need to understand DFT, since they must verify the chip functionality in its test mode. As for design engineers, we see that users of our Design Compiler tool—traditional logic-design engineers—also run DFT Compiler and DFT MAX, our scanning and compression tools. We've made these tools part of the design flow, so these engineers don't have to call in test experts.

What impact is growing IC complexity having on test?

One example is that you can have a path with no defects from the standpoint of functional failure. An increased resistance on a via will make the node switch, but the delay is going to be much longer, resulting in a small delay defect. Another growing concern is power consumption. As engineers reduce power consumption on chips, they are designing thinner power and ground lines. As a result, testing can stress the chip with an amount of switching that can cause a failure. So, a new challenge is how to keep the pattern count low and the coverage high while reducing power consumption.

What are your key tools for addressing new test challenges?

A very important one is DFT MAX. It automatically implements "adaptive scan," the Synopsys version of scan-compression, on-chip hardware, to reduce the amount of test data. Companies need this technology for two reasons: First, testers have a finite amount of memory to retain test patterns, and, second, customers want to limit the time spent by the tester on each device. If test patterns exceed the tester-memory limit, they are cut back, which lowers test quality, ultimately resulting in higher service costs. You can add more memory, but [doing so] increases costs. At our recent San Jose user conference, RFMD reported projected savings of $25 million from using DFT MAX.

How about improvements in ATPG (automatic test-pattern generation)?

Advanced fault models are driving ATPG to produce higher test quality. For example, small delay defects associated with nanometer processes can adversely affect timing-sensitive paths, leading to circuit failures. Standard transition-delay ATPG lacks sufficient timing resolution to create tests that reliably detect these small delays. The Synopsys TetraMAX solution, however, can process precise timing information from the PrimeTime suite to generate small delay-defect patterns and identify subtle defects that were previously undetectable.

What will be your future key focus in DFT technology?

Early this year, we announced that our IC Compiler was used in a 45-nm system-on-chip device from Matsushita. The size of this chip was over 250 million transistors. So, customers clearly are planning larger designs. This [situation] means we'll need to make more strides in compression to extend tester life. More gates on the chip also require greater capacity and faster run time, which we're addressing in all our tools, including test. Customers want to reduce power in test-pattern generation. As we move to smaller chip geometries, such as 32 nm, we'll need to respond to defects related to small delays and other issues. Finally, there's the challenge of design flow. For example, the more compression you do, the more problems you have in place and route because of more congested circuitry. We must always make sure that overall design productivity is not compromised by test requirements.

—Lawrence D Maloney

ON EDN.com:
Antun Domic addresses more questions on DFT, including regional needs among engineers, in the online version of this interview at **www.edn.com/innovate0826**.