> TSMC / JACK SUN

Helping chip design and PROCESS DEVELOPMENT MOVE FORWARD

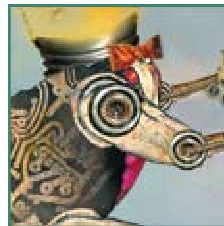
TSMC's vice president of research and development, Jack Sun, looks at the future of foundry/design-team relationships.

AS THE PIVOTAL PLAYER in the CMOS-foundry industry, TSMC (Taiwan Semiconductor Manufacturing Co) occupies the leading edge not only in advanced-process market share, but in process development and the rapidly evolving art of building relationships between foundry engineers and chip-design teams. TSMC's vice president of research and development, Jack Sun, is in the perfect place to watch both parties in this increasingly complex dance as they strive to outmaneuver the growing complexity of CMOS processes. *EDN* asked Sun what he sees as the foremost problem facing the foundry-design relationship today.

Sun answered quickly. "The primary problem today, as we take 40 nm into production, is variability," he says. "There is only so much the process engineers can do to reduce process-based variations in critical quantities. We can characterize the variations, and, in fact, we have very good models today. But they are time-consuming models to use. So, most of our customers still don't use statistical-design techniques. That means, unavoidably, that we must leave some performance on the table."

Sun went on to describe a number of measures that TSMC engineers and customers are taking to reduce the amount of performance chip designers must give up to guard-banding. To begin with, he says, TSMC has consistently made decisions in choosing its process architectures to make things simpler for chip designers. One such decision was the choice—despite considerable capital and development investment—to move to immersion lithography. Immersion has significant benefits for the foundry. But it also means that TSMC can deliver—other variables being equal—more consistent shapes and accurate lithography simulation. "We can pretty accurately predict the actual shapes of features on the silicon now," Sun says. "That means that extraction tools can more accurately predict transistor performance [and] circuit and parasitic impedances. And we don't have to leave too much on the table to allow for unexpected variations in shapes and dimensions."

Another key choice, Sun maintains, was the decision to stay with a conventional silicon-gate, silicon-oxide-dielectric gate stack. "We were able to stay with a structure our customers are used to," Sun says, "and still achieve leadership in power density. Our non-high-k process is rivaling competitive high-k processes."



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But this choice meant that the foundry had to take other steps to increase performance. Sun says that the 40-nm process required scrupulous design work to eliminate excess gate capacitance, further wrestling with contact resistance, and a substantial increase in strain on the channels. "At this point, we are about running out of room for strain structures on the transistor," Sun admits. Feature density and the fact that the impact of strain on channel mobility is orientation-dependent have required TSMC to require fixed-pitch patterns in dense areas and to enforce unidirectional channel orientation.

Another key area in making the process usable for chip designers is modeling—creating not just accurate models, but also the process controls that reduce variations enough to make the models meaningful. Sun says that baseline transistor models are still adequate—at least for the 40-nm, baseline transistor models. Substrate modeling, however, creates extremely complex nets and requires a huge amount of silicon validation, making it a more complex issue.

Sun highlights the issue of advanced process controls. "TSMC uses both feedback and feedforward control loops and gathers a huge amount of data. We do a lot of, if you will, data mining to find the best knobs to tweak to control process variables," he says. "We have so much experience with this now that we are tantalizingly close to being able to do an expert system for process centering." In one case, TSMC had established an integrated link between its advanced process-control system and the chip-design partner's database. "It's a new concept we are trying," he explains. "For most

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partners, we provide data in the form of process sensitivities, so the partners can update their test procedures to look for the things that we know can vary."

In the absence of statistical tools, TSMC must also work to develop process corners that accurately reflect the vastly more complex patterns of variations happening across wafer lots. "We try to find ways to lump parameters together to simplify the corners," Sun says. "But there are, for instance, layout-dependent stress effects. It's a pain you have to live with. The best we can do is to provide accurate Spice models and restrictive design rules that will reduce the variations."

The ultimate weapon in controlling process variations, Sun emphasizes, is not some magic bullet to make the variations go away or magic tool to make them invisible but, rather, a close partnership with design teams to allow them to design with the variations.

"Early adopters—companies like Qualcomm and Altera, which are already on 40 nm—have very early and deep collaboration with the process team," Sun says. "As the process matures, we see a second wave of design teams. These teams still require collaboration, maybe for specific customized features, but otherwise they are working with a proven process and far less uncertainty."

Even though this phased approach describes most collaborations, RF and precision analog designs still represent something of an exception. "RF and analog design have art to them," he says. "The degree of collaboration that actually happens between the design team and its foundry depends on the sensitivity of the design team." Some designers want all the help they can get, Sun suggests, whereas others don't want anyone from outside the team to see—let alone participate in—what is happening within the design team's inner circle. "This [reluctance] can really hinder collective learning," Sun says, "but you have to respect the needs of the designers for differentiation. I think, though, that there is room to improve the model while respecting that. A lot of designers have their own secret sauce. But if the collaboration is not open, you end up leaving the optimizations undone."

—Ron Wilson