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Simple fixture statically tests programmable-gain amplifiers

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The advent of instrumentation amplifiers with digital gain switching offers obvious advantages, such as board-space saving, higher reliability because of fewer solder joints, and lower total cost. These valuable features stem from the fact that the gain-setting networks are integral parts of the monolithic ICs. This feature makes these IC amplifiers much less sensitive to stray electromagnetic fields because the area of internal resistors is a negligible fraction of the previously used discrete gain-setting resistors. Moreover, the value of the relative permittivity of the plastic package and that of the silicon chip are higher than that of the air. As a consequence, the field strength of the electrical component of any stray field penetrating into the chip is lower than that in the surroundings.

Because the gain-setting circuitry is inaccessible directly, a digitally gain-programmable amplifier is a black box. However, the simple fixture in **Figure 1** can help to evaluate some of the static characteristics of these ICs. The fixture comprises Analog Devices' (www.analog.com) 10V REF01 voltage-reference cell, IC_1, the elderly but still excellent industry standard, and a high-precision fixed resistive divider. These components provide a millivolt-range output voltage.

Multiplying the ratio of the resistive divider by the maximum voltage gain of the tested programmable-gain amplifier should give a value of one. The circuit uses tablet-type film resistors having tolerances of 0.1% maximum, yielding a voltage of 10.02 mV at the output of the divider. The two gain-setting logic inputs of the DUT (device under test), an Analog Devices AD8253, connect to short-stranded conductors, which gold-plated pins terminate. Resistors R_{F1} and R_{F2} force the logic level at gain-programming inputs A_0 and A_1 to be low when you disconnect these pins. To set a high level on either or both pins, insert them into the gold-plated counterparts. Two such counterparts interconnect mechanically and elec-

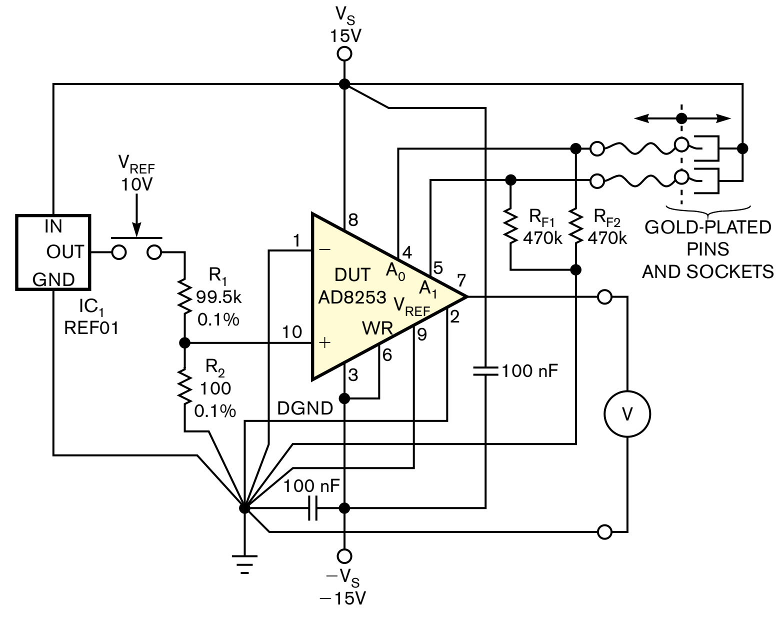

Figure 1 Comprising a handful of components, this circuit allows you to perform your own, independent testing of basic static properties of digitally gain-programmable amplifiers.

trically and remain at the V_S potential. The DUT uses all permutations of the binary values at A_0 and A_1 logic (**Reference 1**). The corresponding voltage gains are one, 10, 100, and 1000.

The evaluation procedure involves measuring the output voltage of the DUT with resistor R_1 both connecting to and disconnecting from the output of IC_1. Thus, you obtain an output voltage of the gain times 10.02 mV and 0V for all voltage gains. The 0V output voltage has a nonzero value because of the input-voltage offset; this voltage might seem high at first glance. However, any fraction of a millivolt of the input-voltage offset times a gain of 1000 yields a fraction of a volt at the output.

When you calculate the differences of the 10.02-mV and 0V output voltages for the respective values of gain, you get a pleasant surprise: These values differ from the ideal values of 10.02 mV times the gain by less than 0.05%. Using this test, you can confirm the precision of the laser-trimmed gain settings. The relatively low value of R_2 ensures that the additional input-offset error arising from input bias current of the DUT has a value of less than 3 μV, whereas the typical value is 0.5 μV. Because proper grounding is an absolute necessity when dealing with tens-of-millivolts scale and high-voltage gains, you must connect supply grounds, digital ground, and other rough grounds with the fine signal grounds in one common junction. **Figure 1** illustrates this approach by using unusual slanted lines for grounding leads.**EDN**

REFERENCE

1 "AD8253 10 MHz, 20V/μs, G=1, 10, 100, 1000 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, www.analog.com/pr/AD8253.

Control system uses LabView and a PC's parallel port

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The circuit in this Design Idea controls the inbound and outbound traffic of cars in a parking lot. This project uses National Instruments (www.ni.com) LabView as the main programming tool and a PC's parallel port for I/O. Basically, the circuit uses the PC's status port, 379h, as an input for sensors, which a relay isolates to prevent damage on the PC (**Figure 1**). At the data port, 378h, the D0 bit controls a door, D1 is a stop signal, D2 is the go signal, and D3 is an indicator of when the parking lot reaches its limit. All the signals drive PN2222A transistors having an external power supply—in this case, the PC's power supply. In this way, you can use relays as loads and control ac voltage for the traffic lights and door motor. The transistor, which D0 drives, controls a DPDT (double-pole/double-throw) relay to invert the motor's polarity.

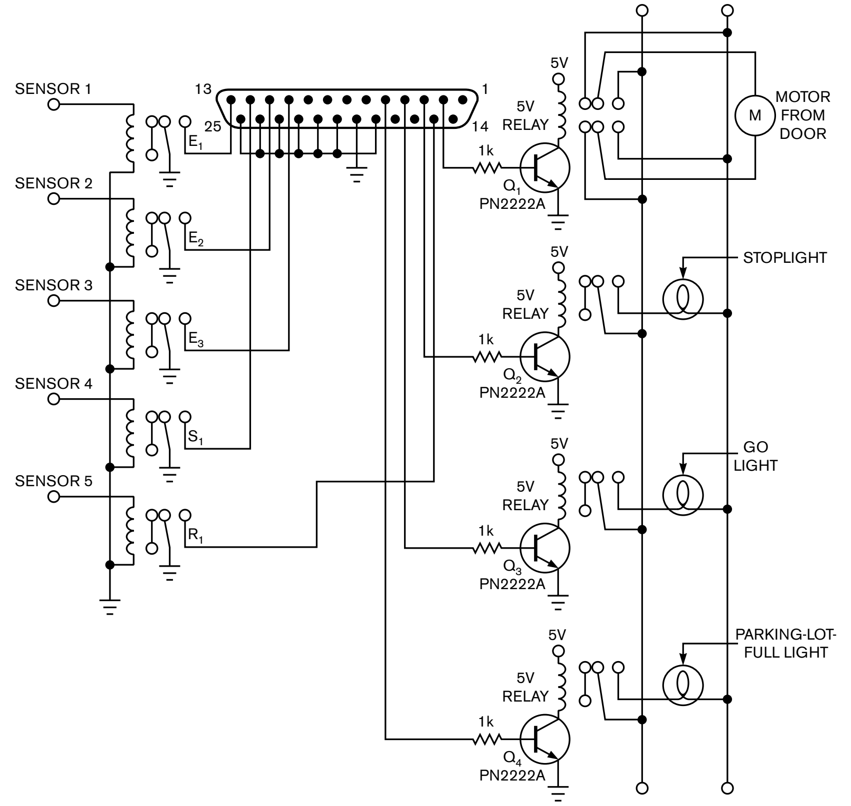

Figure 1 The sensors, indicator lights, and door motor of a parking lot connect through relays to the parallel port of a PC.

Figure 2 shows the LabView diagrammatic program for controlling the parking lot. The VI (virtual instrument) in **Figure 3a** changes the inputs to a low state because all inputs are high by default inside the status register. All inputs have a low state when you do not ac-

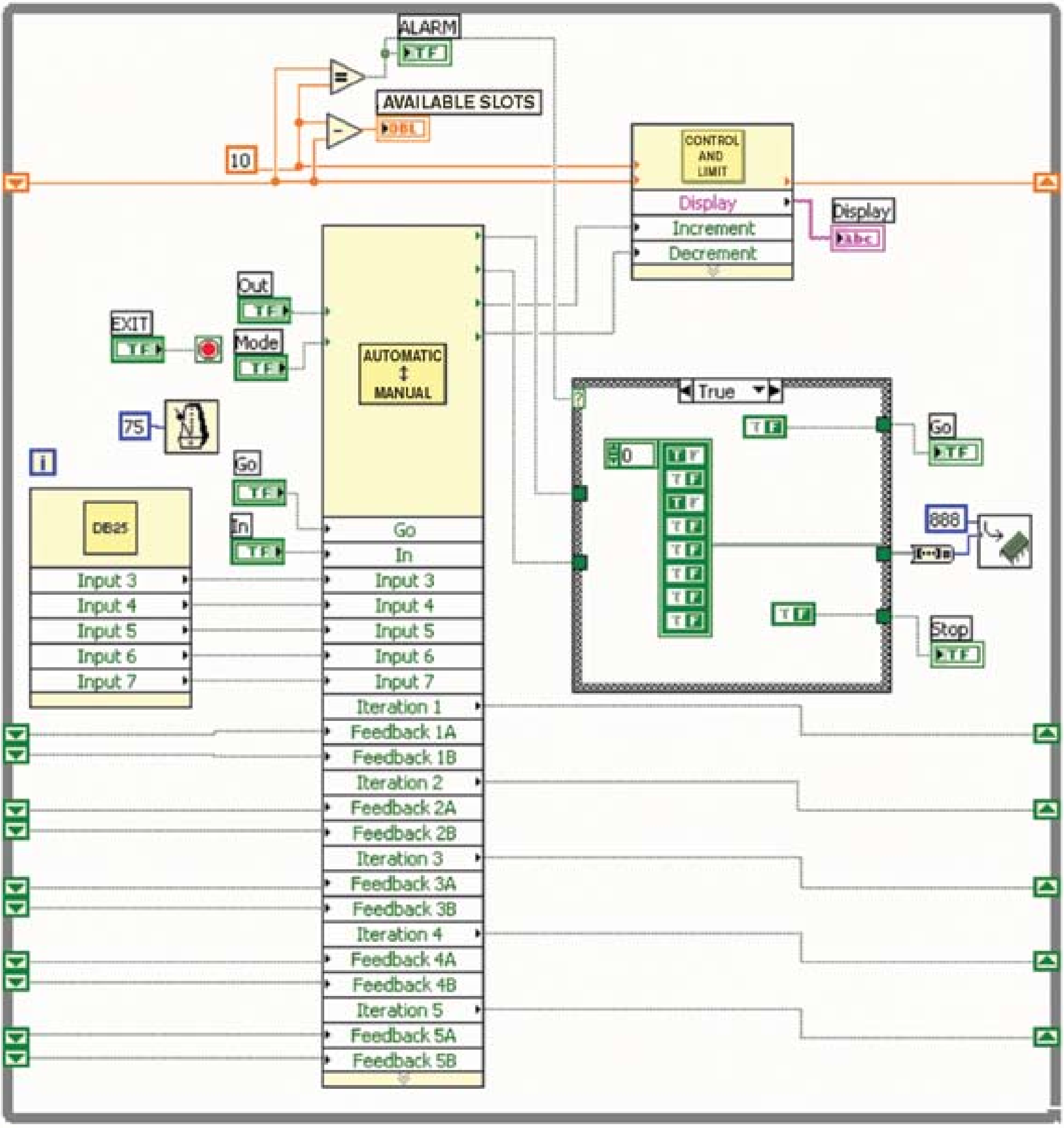

Figure 2 This LabView VI (virtual instrument) controls the operation of a parking lot.

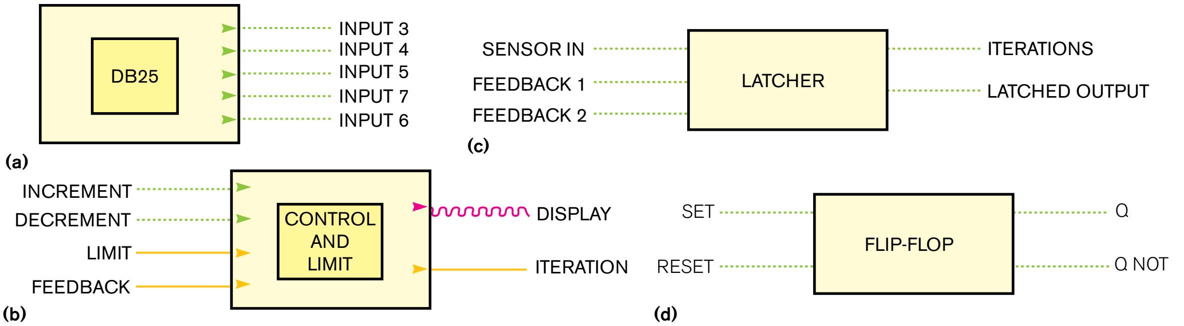

Figure 3 These VIs change the inputs to a low state (a), determine a limit for the number of cars in the parking lot (b), work as a latch-on-release circuit (c), and act as a flip-flop (d).

tivate the sensors. The VI in **Figure 3b** determines a limit for the parking lot, allowing incrementing and decrementing the number of cars parked. This VI also drives a user-oriented display and the shift-register connectors, feedback and iteration, on a "while" loop. The VI in **Figure 3c** works as a latch-on-release circuit; it generates a pulse upon an iteration when the circuit releases the high state on any of the input signals. The VI in **Figure 3d** works as a flip-flop. The VI in **Figure 4** allows switching from automatic to manual mode. Feedback and iteration terminals connect to shift registers, so the latches and the flip-flops inside the VI work correctly.EDN

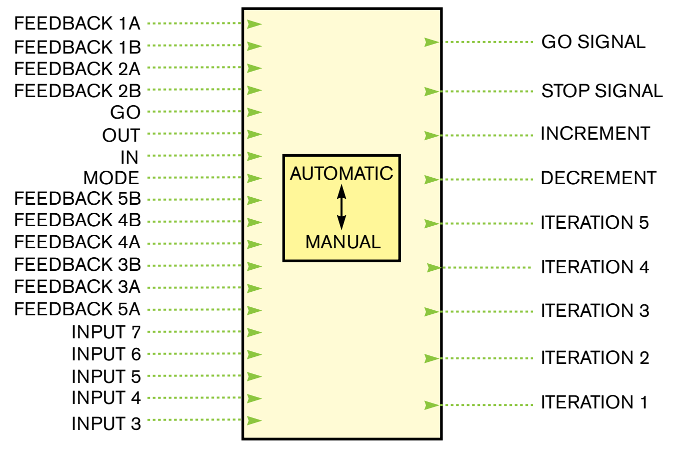

Figure 4 This VI allows switching from automatic to manual mode.

General-purpose components implement USB-based data-acquisition system

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Figure 1 presents a Design Idea for a USB-based data-acquisition system that uses a serial ADC employing general-purpose components, such as D flip-flops, a binary counter, and a shift register. Using the DLP-USB245M FIFO-to-USB-converter module from DLP Design (www.

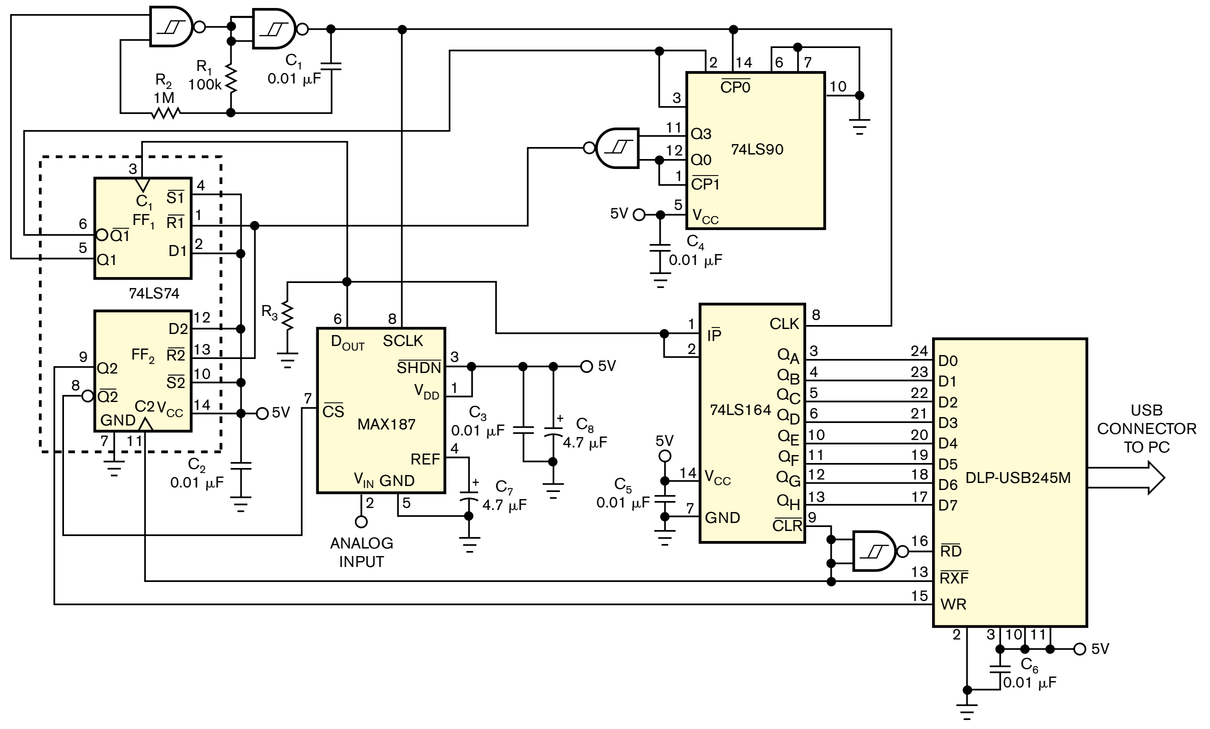

Figure 1 This circuit performs a serial-to-parallel conversion of serial-ADC data and transfers the data to the USB port of a PC.

dlpdesign.com), you can communicate with the peripheral device through the USB port of a host computer. You can write your own program to read and write the data through this module or simply download free test-application software available from DLP's Web site. Additionally, you could download National Instruments' (www.ni.com) LabView serial-read and-write VIs (virtual instruments).

Writing a dummy block of data from the host computer to the buffer of the DLP-USB245M generates a spike at the module's $\overline{RXF}$ pin, which triggers the D flip-flop, FF$_2$ of the 74LS74. The flip-flop's $\overline{Q2}$ pin initiates the conversion cycle of the MAX187 serial ADC from Maxim (www.maxim-ic.com) by pulling down its chip-select pin. The ADC's end-of-conversion cycle causes a low-to-high transition from its D$_{OUT}$ pin, which triggers the other D flip-flop, FF$_1$ of the 74LS74, to generate a gating pulse, Q1, for the serial-clock pulses that read the data from the same D$_{OUT}$ pin of the ADC. The 74LS90 binary counter counts the serial-clock pulses. When the count reaches nine, the counter resets the gating pulse for the serial clock and pushes back the chip-select signal to a high level by resetting both FF$_1$ and FF$_2$, ending the ADC's acquisition cycle.

YOU CAN WRITE YOUR OWN PROGRAM TO READ AND WRITE THE DATA THROUGH THIS MODULE.

The system acquires the data at the falling edge of the MAX187's SCLK pin and shifts it into the 74LS164 serial-to-parallel shift register at the rising edge of the next SCLK. The MAX187 needs nine serial-clock pulses to shift valid 8-bit data. This circuit uses only 8 bits of the 12-bit ADC. If the circuit requires all 12 bits, then you must connect all NAND gates at the appropriate outputs of the binary counter to generate a reset signal by its 13th clock pulse, and you must make the shift register larger.

The serial data from the ADC converts to parallel data in the serial-to-parallel shift register; a WR (write) signal to the DLP-USB245M then transfers this data to the PC. This action is a complement of the $\overline{CS}$ signal from $\overline{Q2}$ of the 74LS74. The DLP-USB245M's $\overline{RXF}$ pin generates a trigger to initiate the conversion cycle and clears the previous data of the shift register.**EDN**

Small, simple, high-voltage supply features single IC

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Sensors, electrostatic traps, and other applications require regulated, high-voltage power supplies that deliver modest amounts of output current. Simplicity, low quiescent current, and compactness are desirable in such supplies. The circuit of **Figure 1** meets these requirements, and its magnetically isolated output allows you to configure a positive, negative, or floating output. A separate winding that generates a feedback voltage proportional to the output voltage, but lower, enables the floating output. This arrangement eliminates the need for high-value resistors in a resistive-feedback divider, which the circuit would otherwise require for direct sampling of the high-voltage output. This low-voltage divider contains resistors with much lower values, which dissipate much less power.

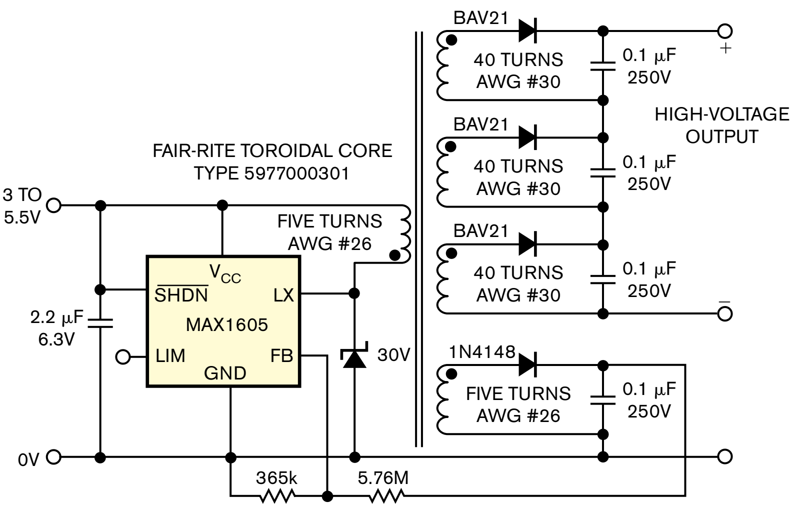

Figure 1 Obtaining feedback from a low-voltage secondary winding, this high-voltage supply generates 500V with low quiescent current.

The MAX1605 IC from Maxim (www.maxim-ic.com) contains the necessary switching regulator, modulator, error amplifier, and power switches (**Reference 1**). It drives the primary of a toroidal transformer that includes a feedback secondary and several output windings. With the component values in the **figure**, the circuit can generate 500V (**figures 2** and **3**). You can vary the output voltage ±30% by adjust-

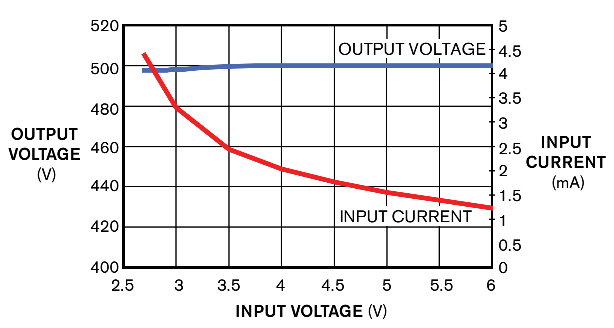

Figure 2 The graph shows output voltage and input current versus input voltage.

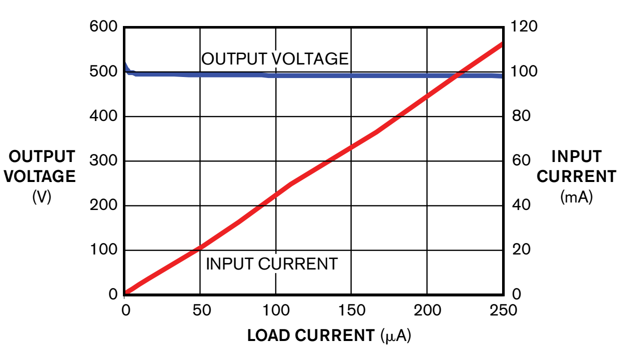

Figure 3 The graph shows output voltage and input current versus load current.

ing the ratio of the resistive-feedback divider. You can also increase or decrease the output voltage in steps by adding or removing the rectifier/capacitor/output-winding modules. The BAV21 is a high-voltage, low-reverse-current, general-purpose diode.

As with all switching converters, EMI (electromagnetic interference) and circuit parasitics can present problems. The circuit needs careful PCB (printed-circuit-board) layout, along with filtering, decoupling, and shielding. The high-voltage output has approximately 1% ripple. You can add an RC or an LC filter in series with the output to achieve lower output ripple.EDN

REFERENCE

1 “30V Internal Switch LCD Bias Supply,” MAX1605 data sheet, Maxim, October 2003, http://datasheets.maxim-ic.com/en/ds/MAX1605.pdf.

CMOS DACs act as digitally controlled voltage dividers

John Wynne and Liam Riordan, Analog Devices, Limerick, Ireland

Digital potentiometers, such as Analog Devices' (www.analog.com) AD5160, make excellent digitally controlled voltage dividers in applications in which 8-bit resolution is acceptable. This Design Idea shows how to use a CMOS DAC as a voltage divider in applications requiring higher resolution.

Millions of CMOS R2R (resistor/two-resistor)-ladder DACs have found use in attenuator applications in which an external op amp acting as a current-to-voltage converter forces one current-output terminal to a virtual ground. The reference input to the DAC can be ac or dc as long as the op amp can produce the desired output voltage. A phase inversion is normal between input and output, so the circuit requires dual power supplies.

Figure 1 shows a way to rewire this simple circuit to avoid the phase inversion and to operate with a single supply. In this configuration, the DAC acts as a digitally programmable resistor, and the DAC's code changes the effective resistance between the input voltage and the I_{OUT1} output-current terminal of the DAC. **Figure 2** shows a practical implementation using one-half of an Analog Devices AD5415 dual 12-bit current-output DAC operating as a voltage divider. This **figure** omits the DAC's control lines for clarity. Op amp A_1 forces the voltage on the I_{OUT2A} output-current terminal to follow the voltage on the I_{OUT1A} output-current terminal. This approach prevents a voltage differential from developing between these two bus lines, which would result in the application of different gate-source voltages across the internal DAC switches and a deterioration in the DAC linearity.

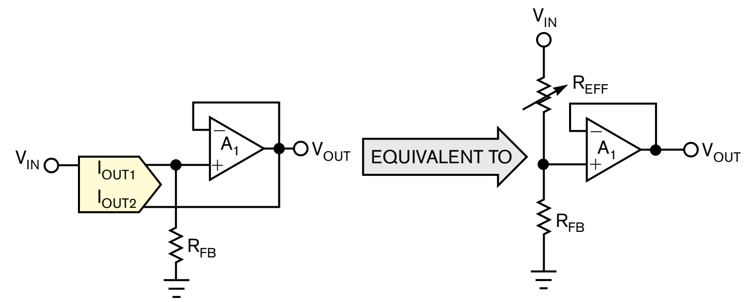

Figure 1 This simple circuit avoids a phase inversion and operates with a single supply. In this configuration, the DAC acts as a digitally programmable resistor.

Wire the split-feedback resistors, R_{FB} and R_1, to produce a composite-feedback resistor equal in value to the DAC's ladder impedance, R. For this arrangement the circuit-transfer function is $V_{OUT}/V_{IN}=(R)/(R_{EFF}+R)$, where R_{EFF} is the effective DAC resistance that is under digital control. Its value is $R(2^n)/N$, where n is the resolution of the DAC and N is the binary equivalent of the digital-input code. Substituting the second **equation** into the first and assuming zero DAC gain error, the circuit-transfer function for a 12-bit DAC reduces to $V_{OUT}/V_{IN}=1/(1+4096/N)$. With all switches off, the effective impedance between the reference voltage and the I_{OUT1A} terminal is infinite, so the output voltage starts at 0V when you load zeros into the DAC. The output voltage increases linearly with increasing code, ideally to approximately half the input with all ones applied to the DAC.

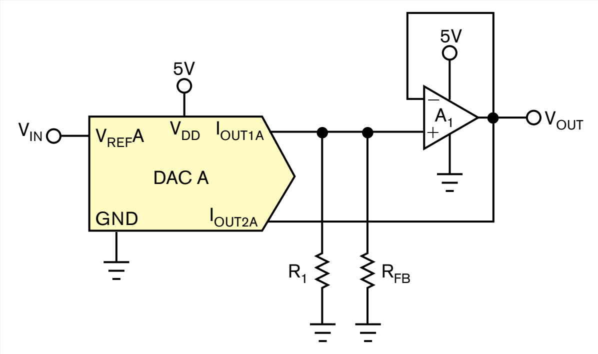

Figure 2 This practical implementation of the circuit in Figure 1 uses one-half of a 12-bit-current-output AD5415 dual DAC that operates as a voltage divider.

The threshold voltage of the DAC's internal N-channel-CMOS switches limits the maximum value of the output voltage, so not all configurations can achieve the full code range. The switch-gate voltage remains at the V_{DD} voltage, and the switch-source voltage rises with the voltage on I_{OUT1A}. As this voltage increases, the on-resistance of the switches becomes large and indeterminate, leading to a flattening of the output voltage and the cessation of the circuit as a predictable voltage divider. For proper operation, the V_{DD} voltage must be a few volts higher than the maximum output voltage—that is, half the input voltage. Otherwise, the input voltage must be less than two times the V_{DD} voltage minus 3V. With a V_{DD} voltage of 5V, the AD5415 operates linearly to approximately a 3.33V output but then flattens. If a wider output-voltage range is necessary, you could use Analog Devices' AD7541A, which uses a 15V power supply, in place of the AD5415. This substitution extends the usable output-signal range to approximately 7V.**EDN**