



BY RICK NELSON, EDITOR-IN-CHIEF

## The design-and-test merger

**A**re the design and test disciplines merging? You might get that impression from reading some recent items in the news. I addressed the design-and-test relationship with an earlier commentary (**Reference 1**). That editorial was a response to an article by Executive Editor Ron Wilson (**Reference 2**). I stand by my March 20 conclusion that “it would be a mistake to assume that embedded instruments will make external instruments go away.” But recent news and events suggest that embedded instruments will continue to make inroads.

First, Asset InterTech ([www.asset-intertech.com](http://www.asset-intertech.com)) announced last month that it is positioning the company, its products, and its technologies to provide open tools for embedded instrumentation in design-validation, test, and debugging applications because, according to Asset President and Chief Executive Officer Glenn Woppman, established validation and test technologies are inadequate for high-speed chips and I/O buses. Chip geometries at 45 nm or smaller, as well as chip-level packaging technologies, such as SIP (system in package), he says, are making validation, test, and debugging difficult if not impossible with traditional technologies.

Embedded instrumentation naturally requires a design element. Instrumentation—in the form of BIST (built-in-self-test) or DFT (design-for-test) structures—won’t get embedded if chip designers don’t do the embedding. Prasad Mantri, a staff engineer at Sun Microsystems who focuses on DFT, commented on that topic in his June 5 presentation during the third annual Global STC (Semiconductor Test Consortium, [www.semitest.org](http://www.semitest.org)) Conference, which took place June 4 through 6 in San Diego. Dur-

ing that presentation, titled “Design for Test: Small Price to Pay on Silicon for High Product Quality,” he said that the high cost of production-worthy ATE (automated test equipment) represents a problem, one that transferring the test function from ATE to the design stage would alleviate—“as if design wasn’t already hard enough.”

Mantri noted that DFT is necessary because of increasing chip complexity: I/O count increases linearly as feature size shrinks, and gate count or flip-flop count increases in a squared relationship with feature-size shrinkage. He added that the DFT process has become as complex as any other part of the electronic-design-automation flow. DFT insertion is no longer accomplished using point tools after designers complete a design through gate simulation and then “throw it over the wall” to the DFT engineers. In fact, he said, designers are not simply tolerating DFT because it’s part of a design specification; they are also asking for it as an aid to debugging, diagnosis, and field-failure analysis.

Sanjiv Taneja, vice president of the Encounter Test division at Cadence Design Systems ([www.cadence.com](http://www.cadence.com)), also addressed the relationship

between design and test at the STC conference with a presentation titled “Cooperation between EDA and ATE: Now More Important Than Ever.” He said that test and EDA vendors need to look beyond the interoperability issues that they addressed in the 1990s to provide interoptimized, end-to-end technologies. An effective design-and-test strategy, he said, will require a holistic effort across the entire chip-design and -production ecosystem, consisting of ATE, EDA, and semiconductor companies; foundries; assembly-and-test houses; IP (intellectual-property) providers; and even universities.

I think that both Taneja and Mantri would agree with me that external testers are here to stay. In fact, Mantri said he sees a growing role for DFT-focused testers as well as protocol-aware functional testers. He noted that some DFT proponents have tried for many years to put test-equipment vendors out of business. But, he said, addressing the test-equipment-vendor representatives in the STC conference audience, “You guys are still here.”

For more on design and test, see our special issue *Innovators 2008*, particularly the interviews with Antun Domic, a senior vice president and general manager of the implementation group at Synopsys ([www.synopsys.com](http://www.synopsys.com)), and Mike Santori, technology and business fellow at National Instruments ([www.ni.com](http://www.ni.com)). If you don’t have a copy of *Innovators 2008*, please go to [www.edn.com/innovate08](http://www.edn.com/innovate08). **EDN**

### REFERENCES

- 1 Nelson, Rick, “External instruments here to stay,” *EDN*, March 20, 2008, pg 12, [www.edn.com/article/CA6541381](http://www.edn.com/article/CA6541381).
- 2 Wilson, Ron, “As SOCs grow, test-and-measurement instruments move on-chip,” *EDN*, Feb 21, 2008, pg 31, [www.edn.com/article/CA6531583](http://www.edn.com/article/CA6531583).

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