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## Third-party-IP providers: physical-design questions, part two

**E**ngineers often overlook one physical-design issue for qualifying IP (intellectual-property) blocks: handling routing blockages and overlayer-routing conditions. Traditionally, IP designers created blocks with their routing on layers M1 through M3, leaving layers M3 to M6 for block-to-block signals, global routing, clocks, and power supplies. Today's less-than-90-nm processes support as many as 12 layers of metallization,

however, so the guidelines for handling in-block and overblock routing have changed.

Placement-and-routing environments use abstract descriptions of the IP block in LEF (library-exchange-format) and DEF (design-exchange-format) files. These descriptions detail pin locations, types, and layers; the data extent of the IP; power and clock paths; and blockages so that the automatic routers do not use specific wiring channels for interconnect. In older process technologies, designers identified blockages in the LEF and DEF files as paths for the wider power-supply metal, feed-through paths for known block-to-block-interconnect signals in prerouting, or areas for clock-buffer insertion. These blockage identifications occurred only on the M1 through M3 layers and dealt only with the placement of wires.

The abstract descriptions of the blocks for both primitives and higher functions contain no instructions about how interconnect layers above the block should behave. The only mechanism for controlling routing in the higher metal layers is the ability to add a blockage if necessary. Modern processes with many intercon-

nects and those using advanced CMP (chemical-mechanical polishing) also have nonwiring and wire-class-blockage requirements.

Examples of nonwiring blockages are those for minimum square-metal fill on certain layers, identification of where to place fill to accommodate wire spreading, spacing regions for OPC (optical-proximity-correction) and PSM (phase-shift-mask) artifacts, BIST (built-in-self-test) regions, indie-pad regions, and TSV (through-silicon-via) targets. These blockages reside on layers, such as metal layers M4 through M12, where there is no data. Designs can now require clock-, power-supply-, and power-down-class wire-class blockages. Most of the current SOC (system-on-chip) designs use multiple clock domains. Special-function IP may have a large disparity between its operating frequency and the high-frequency clocks running some of the I/Os, memory, and datapath blocks.

Because the layers above the IP block require metal fill for CMP, a source of coupling from multiple layers results from these clocks and signals in the IP. Identifying clock-class blockages is a method of isolating har-

monics that the interaction of these multiple clock frequencies causes, preventing them from causing non-buffer-related clock skew.

To build electronic systems with multiple functions, the SOCs rely on multiple power supplies to build the application-specific modules. As a result, even small to midsized designs commonly have two or more power-supply and signal levels. The lower-voltage cells have necessarily scaled-down switching levels with increased sensitivity to noise and to false switching. This sensitivity results from the simultaneous switching of signals on other higher-voltage pairs. Identifying power-supply-class blockages clears sensitive areas of overblock signals that could cause false switching and increased ground noise. This precaution is key to maintaining signal integrity in the design, and it is necessary to any design-verification strategy.

Similar to the power-supply blockages, SOC designs have multiple power-operation modes. In the reduced-power states, techniques such as the use of retention registers or multithreshold logic ensure that the block returns to proper operation. However, using these techniques can incur the risk of false data registration due to noise from switching signals in overblock routing during the power-supply restoration. To minimize this hazard, designers should identify blockage areas so that this large-signal coupling cannot take place.

It is important to verify that any IP, especially for less-than-180-nm processes, includes application-based blockages, such as those described, so that a parametric-driven physical-design flow can complete its task, giving you a high degree of confidence. **EDN**

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