



BY BONNIE BAKER



“Muxing” around with delta-sigma converters

A multiplexer in your circuit can scan through a number of input channels by sampling each channel in rotation. As a power and cost advantage, multiplexed systems have only one ADC that acquires the data from all of the channels. Before starting your design, first look at the types of signals you are trying to digitize. For instance, if you know the highest and lowest frequency as well as the accuracy requirements in all of your system’s channels, you may see a need for several ADCs.

In another scenario, the channels may have a unique time relationship to each other, requiring a simultaneously sampling approach that preserves phase information. You achieve this goal with sample-and-hold circuits and a single ADC, or it may be easier to use individual ADCs.

Figure 1 shows a delta-sigma converter multiplexed circuit with the anti-aliasing filters on the signal side of the multiplexer. Each channel of this circuit has a near-dc signal at the input

of the multiplexed converter. However, a channel-to-channel change can create a step-response signal to the ADC. Thus, it is critical that you use a zero-cycle-latency converter.

Cycle latency is equal to the number of complete data cycles between the initiation of the input signal conversion and the availability of the corresponding output data. The converter must be able to generate a fully settled output signal from a step input. If the device completes the conversion

before the start of the second cycle, the cycle latency is zero. One possible limitation of multiplexed delta-sigma ADCs is a nonzero cycle latency.

Figure 2 shows the signal-chain dynamics of a multiplexed system with three signals. This system links slices from each input channel. After the multiplexer, the zero-latency delta-sigma ADC sees this merged waveform, which has large and fast transitions as the signal switches from channel to channel. The reaction of the delta-sigma converter’s digital filter to the entire multiplexed waveform means that the fast transitions settle completely within the digital filter.

The appropriate delta-sigma-converter class for multiplexed applications performs the conversion task with a zero-cycle-latency characteristic. These delta-sigma converters usually have sinc (sinx/x) digital filters. This class of converter masks internal-digital-filter results from a designer’s view. With a zero-cycle-latency delta-sigma ADC, the first output-data results fully settle.

You can also describe a zero-cycle-latency ADC as having single-cycle settling or a single-cycle conversion. In all cases, however, you will get the right answer from the multiplexed converter the first time. EDN

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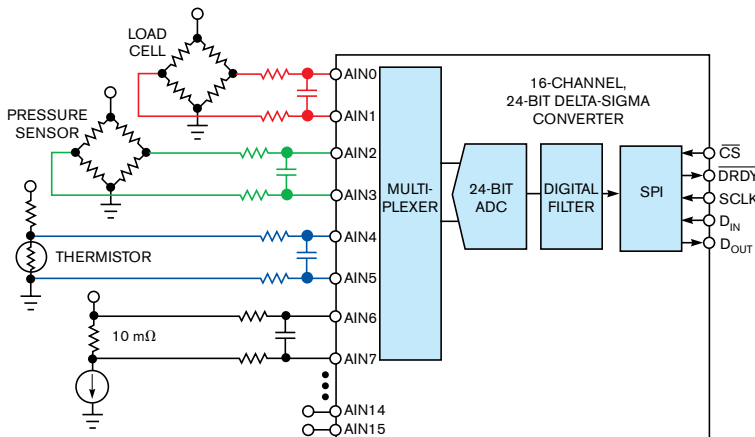


Figure 1 The signal’s frequency content at the input delta-sigma converter is usually slow-moving.

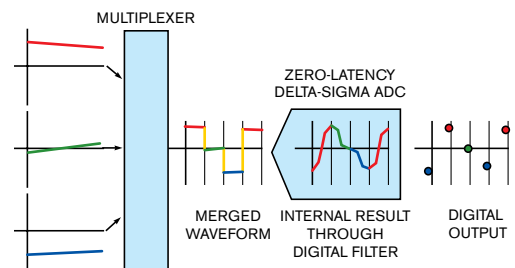


Figure 2 Switching dc signals into the ADC’s input can contain high-frequency components.