High-voltage, high-frequency amplifier drives piezoelectric PVDF transducer

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Piezoelectric transducers find use in NDE (nondestructive-evaluation) applications. The PVDF (polyvinylidene-fluoride) transducer has many advantages, including a wide bandwidth and high sensitivity. These transducers require high-voltage and wide-bandwidth amplifiers. The basis of the circuit in **Figure 1** is an earlier Design Idea (**Reference 1**). The operation of the circuits is basically the same, but this one can drive a 2.3-nF capacitive load at frequencies as high as 500 kHz.

In this circuit, an LM7171 op amp from National Semiconductor (www.national.com) replaces the LF411, also from National Semiconductor, of the earlier design. The LM7171 op amp has a unity-gain bandwidth of 200 MHz. To further improve the bandwidth, this design's mirror circuit uses lower-value resistors to increase the current in the transistors, thus increasing the bias current and the power dissipation of Q_3 and Q_4. To improve thermal stability, this design adds resistors R_{16} and R_{17}, and, to increase the current to drive the transducer's capacitive load, this design adds a current driver to the circuit's output. V_{CC} and V_{EE} are 15 and −15V, respectively, and V_{H+} and V_{H-} are a maximum of 150 and −150V, respectively. EDN

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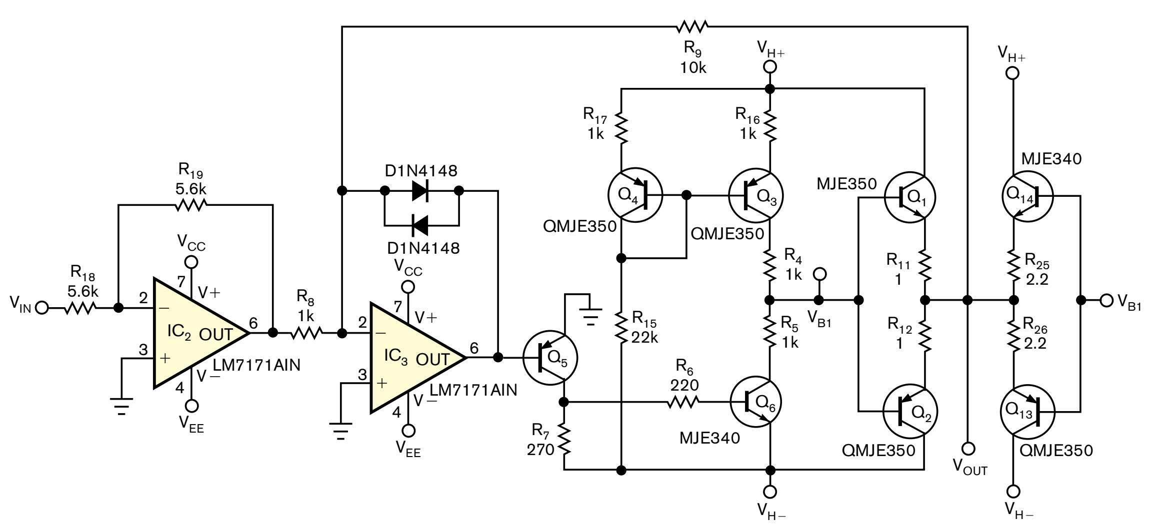

Figure 1 This high-frequency, high-voltage amplifier can drive the capacitive load from a PVDF (polyvinylidene-fluoride) piezoelectric transducer.

Microcontroller detects pulses

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While recently designing an automatic test station employing a microcontroller, I faced a nonstandard task: Detect the presence or the absence of output pulses in the DUT (device under test). You might think this task is easy to accomplish by connecting an LED to the DUT output. The blinking LED provides evidence of the pulse's presence. That approach would work if that test were the only one you needed to perform. In this station, however, the pulse test is just one of more than a dozen tests and measurements. The test station should display the final result—pass or fail—only after completing all the tests. So, it should represent the result of each test in binary format—that is, yes for pass or no for fail. This Design Idea describes a simple way of solving this problem.

The pulses for detection enter the $\overline{IRQ}$ (interrupt-request) pin of the Freescale (www.freescale.com) MC68HRC908JK1 microcontroller (**Figure 1**). Each pulse period is 500 msec, causing an external interrupt. At least three interrupts should occur within 2 seconds. The program waits for 2 seconds, and, if no external interrupts occur during that time, it declares that the pulse test has failed. The red LED on the PB1 pin then switches on, and the test stops. Otherwise, after three interrupts, the program starts the next test. To evaluate the pulse test separately from the rest of the tests, this demo program ends in an indefinite loop instead of starting the next test. When the green LED on the PB0 pin lights up, it indicates that the pulse test has successfully completed. The LEDs work with built-in current-limiting resistors, such as W934GD5V and W934ID5V devices from Kingbright (www.kingbright.com).

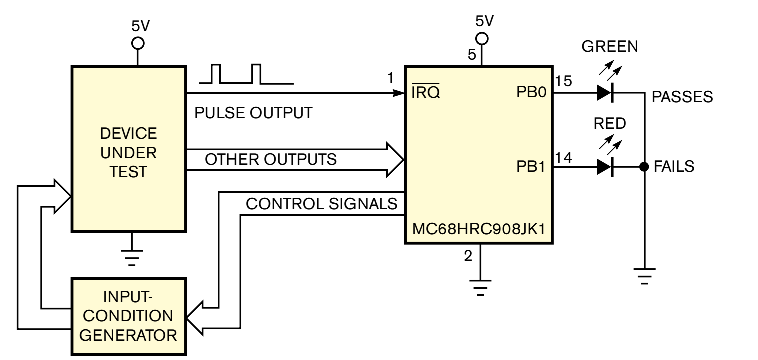

Figure 1 This 8-bit, low-end microcontroller detects pulses from LEDs, yielding a simple tester.

This design uses the low-end, 8-bit MC68HRC908JK1 microcontroller because of its low cost and ability to have 10 8-bit ADC channels. You can find **Listing 1**, the firmware-assembly code for the device, at the Web version of this Design Idea at www.edn.com/080724di1. You calculate the time delay for the oscillation frequency at approximately 4 MHz, which a 20-kΩ resistor and a 10-pF capacitor determine. This approach is applicable to any type of microcontroller because it uses standard assembly instructions. You need to recalculate the time delay only in case of different oscillation frequencies. EDN

Sample-and-hold amplifier holds the difference of two inputs

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You can fulfill a requirement for sampling the difference of two signals in two classic ways. You can subtract the two input signals with an instrumentation amplifier whose output connects to an input of a classic sample-and-hold amplifier. Despite the positive feature of needing no external resistors for a gain-of-one differencing instrumentation amplifier, this approach suffers from high relative output distortion when the inputs are of the same polarity and close in magnitude. In such a case, the difference of two input signals is close to 0V, and the amplifier is therefore more vulnerable to residual dynamic imperfections of the sample-and-hold amp. The other approach is to separately sample the two input voltages in two sample-and-hold amps and subtract the outputs of these amps in an instrumentation amp. Here, the relative error of output signal with similar input waveforms is lower than in the first approach.

If you like all-in-one solutions, you can use the circuit configuration in **Figure 1**. This circuit simultaneously tracks both input voltages, V_{INA} and V_{INB}, at an active-high level of the internal logic-control signal, which enables the A_1, B_1, and A_2 voltage followers. V_{INA} thus appears on capacitor C_2, which is ground-referenced. Capacitor C_1, which is temporarily grounded at its upper node, Pin 9 of IC_1, tracks the V_{INB} voltage. After a settling interval when all of the internal logic-control signals go inactive low, the Q_{SB} logic-control signal goes high. The voltage of $V_{C2}(TS)=V_{INA}(TS)$ shifts the potential at the lower node of capacitor C_1 because of the enabled B_3 follower. Upon the sample command, Q_S is high, and the upper node of C_1 is grounded within the tracking interval. Storage capacitor C_3 therefore charges through the B_2 follower to a voltage of $V_{C2}(TS)-V_{C1}(TS)=V_{INA}(TS)-V_{INB}(TS)$. The A_3 follower serves as an impedance converter.

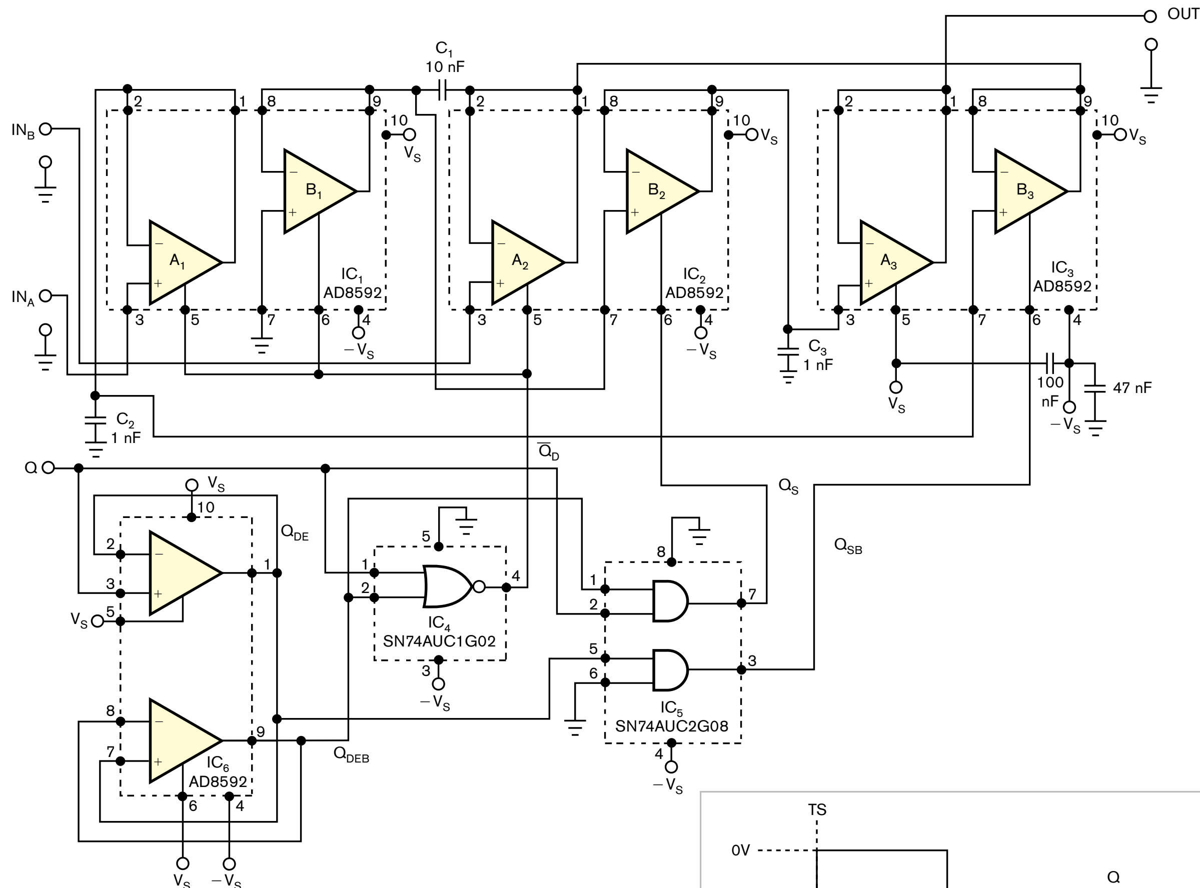

Figure 1 The basis for the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on capacitors C_1 and C_2 and a stacking of these capacitors within the sample interval on capacitor C_3.

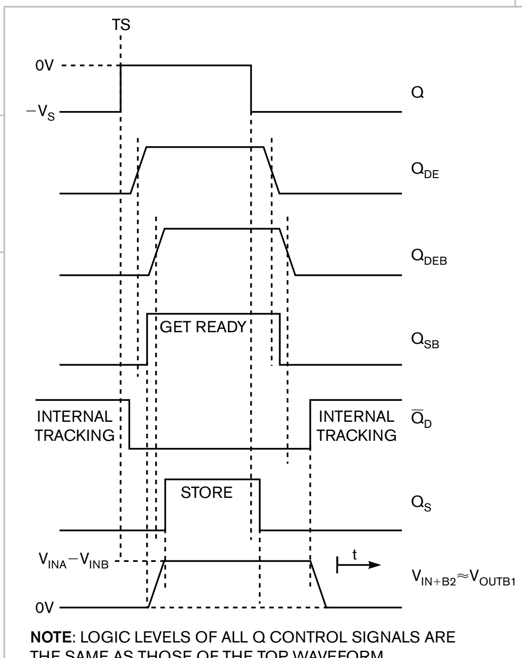

Figure 2 The bottom waveform shows that, at the upper node of capacitor C_1, 0V appears within the tracking interval, and it rises to the value of a difference between both input voltages within the get-ready interval when Q_{SB} is high. The difference of input voltages of $V_{INA}(TS)-V_{INB}(TS)$ resides within the store interval when Q_S is high.

The voltage gains of both the A and the B channels are slightly lower than ideal. This slight gain decrease has approximately the same value for both channels: $\delta_{GAINA}=\delta_{GAINB}\sim(C_{OUTB1}/C_1)$. The equality of gain decrements on both channels stems from the fact that the upper node of the storage capacitor, C_1, connects at the instant that Q_{SB} goes high to the output capacitor, C_{OUTB1}, of the disabled follower, B_1. Follower B_1 always discharges to 0V within the tracking interval without regard to the voltages at the A and B inputs. For Analog Devices' (www.analog.com) AD8592 op amps, the output capacitance, C_{OUT}, in the disabled state is approximately 26.2 pF.

Note, however, that if V_{INA} and V_{INB} are of opposite polarity and of equal magnitude, almost reaching the value of $V_S/2$, the output voltage approaches either the positive- or the negative-supply rail. In this case, the relative output error is about twice that given in the previous **equation**. The op amps' capacitance rises as the output voltage approaches any of the supply rails, reaching the value of 55 pF. This increasing output capacitance arises from one of the complementary power transistors in the AD8592's output stage as its drain-to-source voltage approaches 0V at the output voltage close to the positive-supply rail. The increasing drain-to-source capacitance with decreasing drain-to-source voltage is an inherent property of MOSFET transistors. The same situation holds true for the bottom power transistor of the AD8592's output stage, when the output voltage approaches the negative-supply rail.

The turn-on time of the AD8592 is much longer than the turn-off time. Although the device's data sheet does not directly specify these times, you can see from the internal structure of the IC that the on/off control enters almost all of the IC's stages (**Reference 1**). Thus, turn-off is fast because the turn-off of the output stage occurs without regard for the states of the preceding stages.

Within one period of operation of the circuit in **Figure 1**, a sequence of two turn-ons (T_{ON}) plus four intentionally added delays (T_{DE}) determines the shortest sampling period: T_{MIN}~T_{ONB3}+$4T_{DE}$+$T_{ONA1B1A2}$. Here, $T_{ONA1B1A2}$ is the largest from among the values of turn-on times of followers A_1, B_1, and A_2, which depend on the actual values of V_{INA} and V_{INB}. The maximum sampling frequency is then $1/2(T_{ON}+2T_{DE})$.

If you assume that the maximum turn-on time can reach the value of the overvoltage-recovery time of approximately 3 μsec and that the delay time is approximately 0.35 μsec, then it follows that the maximum sampling frequency is approximately 135 kHz. The duty-factor of the external logic-control signal, Q, for sampling frequencies near the value of the maximum sampling frequency should be about 0.5 (**Figure 2**).EDN

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Precision capacitive-sensor interface suits miniature instruments

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In some applications of capacitive sensors, the instrument's front end must be small enough to fit into a narrow space. **Figure 1** shows a precision capacitive-sensor interface for such use. The square-wave output from a low-voltage 555 timer, IC_1, constantly triggers the precision one-shot, IC_2, to produce quasistable outputs for time periods T_1 and T_2, which are proportional to external timing capacitance: $T_1=KR_0(C_S+C_0)$, and $T_2=KR_0C_S$, where K is the multiplier factor. K is nearly independent of the external timing capacitance when that capacitance is more than 100 pF (**Reference 1**). So, a 150-pF capacitor, C_0, in shunt with the capacitive sensor, C_S, supplies an offset so that operation of the one-shot remains within a linear range even if the value of C_S is less than 100 pF.

To achieve good measurement accuracy, connect a reference channel with a fixed 150-pF capacitor. This method cancels the effects of both stray capacitance and transition time. A single 3.3V supply powers this interface circuit. The circuit's compact design permits flexibility, and you can easily

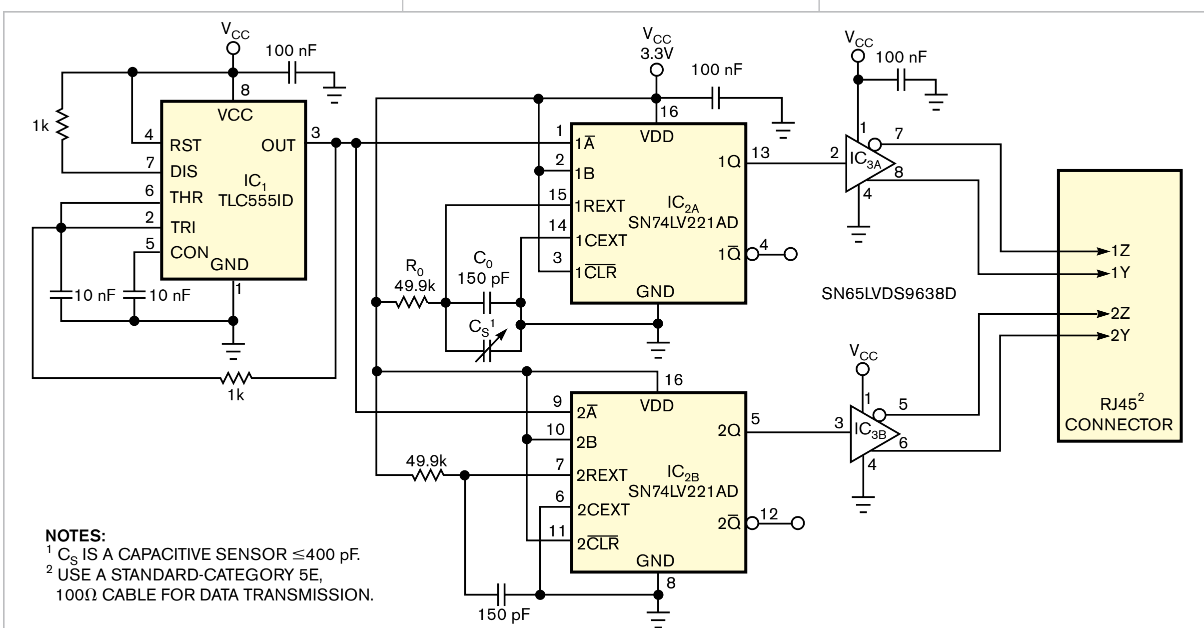

Figure 1 This compact capacitive-sensor-interface-circuit design permits great flexibility; you can easily integrate it into a miniature sensor head near the measurement point.

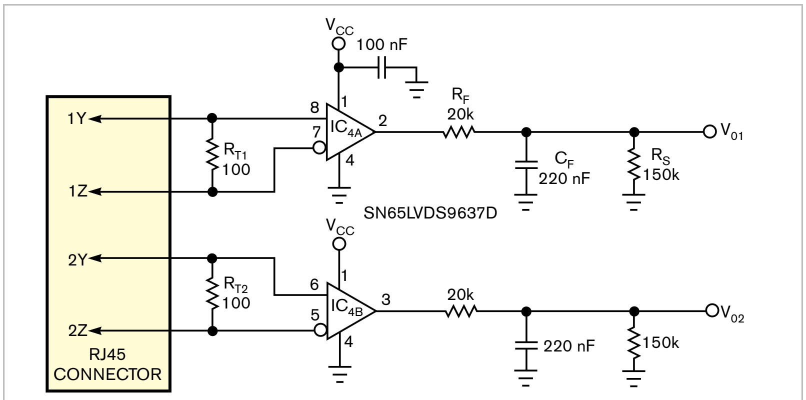

Figure 2 At the terminal, IC_4 converts the signals it receives from the interface to LVTTL levels and then feeds them to a set of passive filters.

integrate the circuit into a miniature sensor head near the measuring point. IC_3 converts the outputs to LVDS (low-voltage-differential-signaling) levels and then transmits these outputs using a standard Category 5e cable to the terminal, which may be some distance away. As long as the cable is shorter than 10m, the transmission bandwidth is adequate for ensuring acceptable measurement accuracy within several picofarads to hundreds of picofarads (**Reference 2**). In **Figure 2**, the terminal at IC_4 converts the signals it receives from the interface to LVTTL (low-voltage-transistor-to-transistor-logic) levels and then feeds them to a set of passive filters. Each dc output is proportional to the signal's duty cycle:

$$V_{O1} = V_H \times \frac{T_1}{T_P} \times \frac{R_s}{R_f + R_s},$$

and

$$V_{O2} = V_H \times \frac{T_2}{T_P} \times \frac{R_s}{R_f + R_s},$$

where V_H is the high-level output voltage of IC_4 and T_P is IC_1's oscillation period. By digitizing the two outputs, you can obtain a reading proportional to the sensor's capacitance, $V_{O1} - V_{O2}$. Be sure that $T_1 < T_P$—that is, $C_S < T_P/(K \times R_0) - C_0$; otherwise, the final output will be erroneous. For the sake of a wide measurement range, keep T_P as long as the target application permits. **EDN**

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