

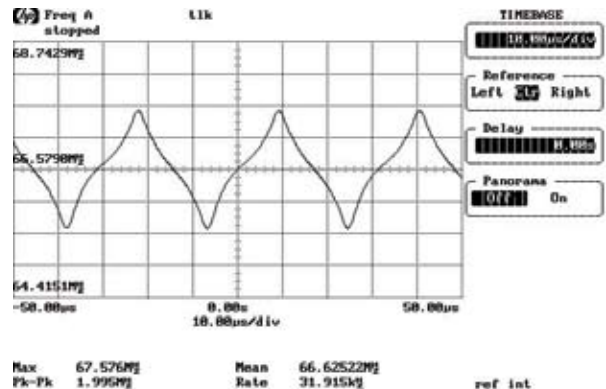
Spread-spectrum-clock generators reduce EMI and signal-integrity problems

AS ELECTRONIC PRODUCTS BECOME FASTER AND MORE COMPLEX, RADIATED-EMI EMISSIONS INCREASE DRAMATICALLY. WITH THE RECENT PROLIFERATION OF PORTABLE AND WIRELESS PRODUCTS, THIS GROWTH HEIGHTENS THE PROBABILITY OF INTERFERENCE BETWEEN SYSTEMS AND MAKES EMI A MAJOR CONCERN.

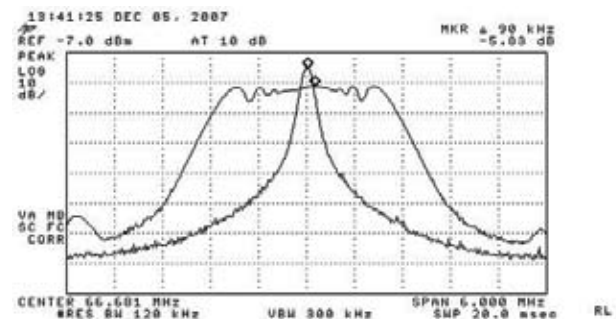
It is well-known that, during system development, critical signal-integrity and EMI (electromagnetic-interference) simulations are difficult, time-consuming, and error-prone due to their reliance on hard-to-predict models and parameter extractions. This situation worsens with every new product generation due to steadily increasing clock speeds and decreasing supply voltages, resulting in reduced noise margins. These problems, coupled with the shorter product-development periods that shorter product-life cycles require, hinder the ability of designers to bring their products to market fast enough to meet market demand. The ever-increasing expectations of the end user or the consumer require approaches to such problems that interfere with a company's ability to expeditiously manufacture quality products at high volumes and to outpace dwindling product life spans in the market.

Although simulating electronics systems to predict EMI levels is a difficult and time-consuming task, understanding the fundamental causes of electromagnetic radiation is simple. Any charge moving in an electrical field or change in a field emits electromagnetic radiation. The strength of radiation is directly proportional to the rate of change. The sources of electromagnetic emissions can be intentional transmitters, such as cellular phones. But digital systems, such as PCs, PDAs (personal digital assistants), printers, and scanners, emit unintentional radiation. In digital systems, periodic clock signals are the major causes of EMI radiation. In addition, control and timing signals, address and data buses, interconnect cables, and connectors also contribute to EMI emissions.

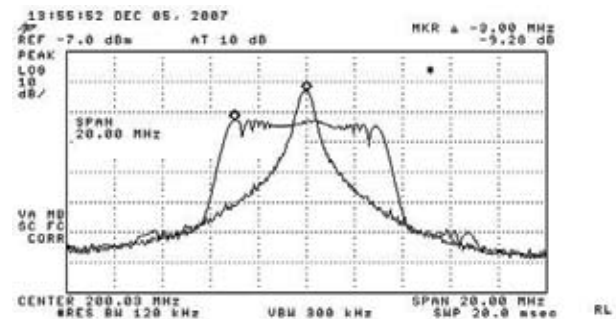
The two main modes of electromagnetic radiation are the differential mode, the result of local current loops between PCB (printed-circuit-board)-interconnect traces and the ground planes, and the common mode, the result of the coupling of ground and power-plane noise into traces, I/O buses, and cable lines. Fundamental and odd multiples of fundamental sinusoidal frequencies, or harmonics, generate a square wave. EMI radiation increases with higher edge speeds (rise and fall times) and higher drive levels. Harmonic frequencies set the exact location of the radiation spectrum and the clock-signal



(a)



(b)



(c)

Figure 1 A Lexmark Profile of a modulated 66.666-MHz system clock (a) shows the relative EMI reduction for fundamental (b) and third-order harmonics (c).

edge speeds, and drive levels set the bandwidth, or radiation strength, of each harmonic.

Shielding is a relatively simple way to reduce EMI emissions by containing them within the system and fully or partially covering the emission locations with grounded conductive shields. Shielding could be an effective approach in systems with strong emissions in which space, weight, and cost are unimportant. In most systems, however, especially portable and handheld products, shielding becomes the least desirable method of EMI reduction. Shielding increases the size, weight, and cost—creating a substantial increase in labor costs, for example, because the shielding of these products is difficult to automate in manufacturing.

Designers widely employ lowpass filters to reduce EMI emissions that clock and timing signals generate. They reduce rise

and fall times by filtering out higher-order harmonics. But this option might not be viable in high-speed systems because such filtering both reduces the critical setup-and-hold-time margins and increases signal overshoot, undershoot, and ringing. A major problem with filtering rests on the fact that this technique is not systemic, meaning that reducing EMI emission at any given node in the system does not reduce the emissions in the other nodes. Because designers start with little information, they must provide filter placement in many suspicious locations, wasting valuable time and PCB space.

SPREAD-SPECTRUM CLOCKS

A more effective and efficient approach is to use SSCG (spread-spectrum-clock generation) to control and reduce EMI emissions. Instead of maintaining a constant frequency, the SSCG technique modulates the system-clock frequency with a much smaller frequency—typically 30 to 90 kHz—to control and reduce EMI emissions at their source, the system clock. The systemic nature of SSCG has a major advantage over other EMI-reduction techniques because all clock and timing signals you derive from the spread-spectrum clock are also modulated at the same percentage, leading to a dramatic EMI reduction throughout the system.

SSCG can reduce the radiated emissions of the digital-clock and -timing signals. You achieve EMI reduction by frequency-modulating the system clock with a low-frequency signal. This approach creates a frequency spectrum with sideband harmonics. Intentionally broadbanding the narrowband repetitive system clock simultaneously reduces the peak spectral energy in both the fundamental and the harmonic frequencies. The MF (modulation frequency) is usually 30 kHz, large enough to stay above the audio band yet small enough to avoid timing and tracking problems in the system—typically at less than 90 kHz.

Figure 1a shows the Lexmark Profile, a typical nonlinear-frequency profile, which Lexmark International patented (Reference 1). In this example, a unique, 32-kHz, nonlinear-frequency profile modulates a 66.666-MHz system clock using $\pm 1.5\%$ frequency-modulation limits. Because the modulation centers on 66.666 MHz, this type of profile is known as center-spread-frequency modulation. Figures 1b and 1c show the amount of relative EMI reduction on the same clock using $\pm 1.5\%$ center spread in reference to an unmodulated system clock for fundamental (b) and third-order (c) harmonics. Figure 2 shows the

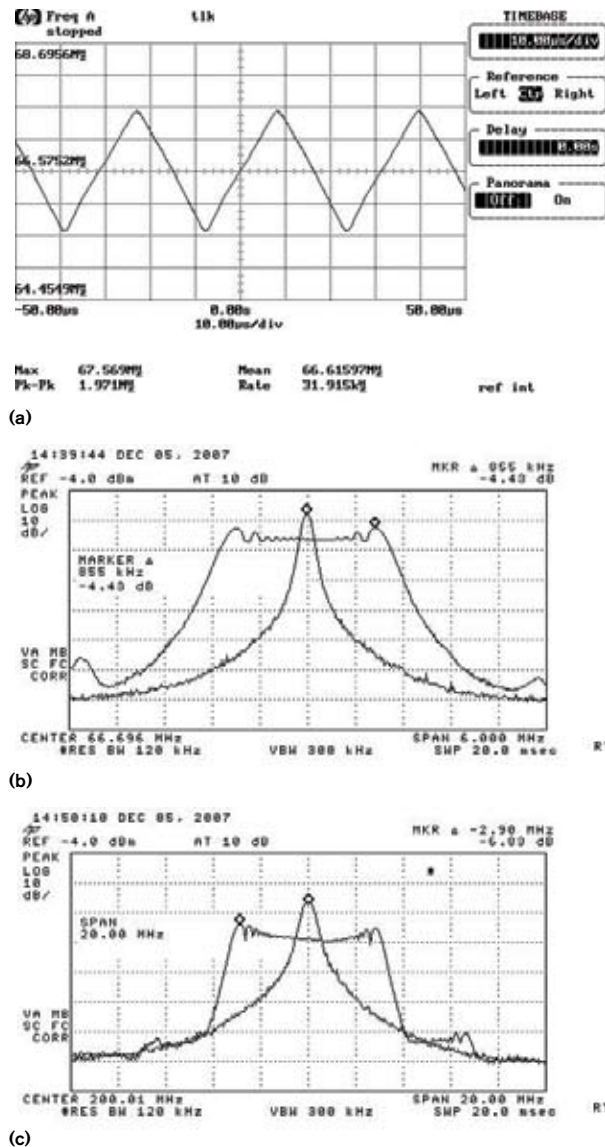


Figure 2 A triangular profile of a 66.666-MHz system clock (a) with a $\pm 1.5\%$ center spread shows similar relative-EMI reductions for fundamental (b) and third-order (c) harmonics.

TABLE 1 PROGRAMMABLE PARAMETERS AND RANGES FOR THE SL15100

Programmable parameter	Range	Resolution
Output-to-output skew (psec)	- 160 to +160	20
Output-drive strength (Ω)	20 to 100	20
Output-rise/fall times (15-pF clock)	0.3 to 4.2 psec	0.3 nsec
Duty cycle (%)	- 3 to +3	1
Frequency	1 to 200 MHz	2 ppm
Spread-spectrum amplitude (%)	0 to 5	0.05
Spread-spectrum modulation (kHz)	16 to 128	1

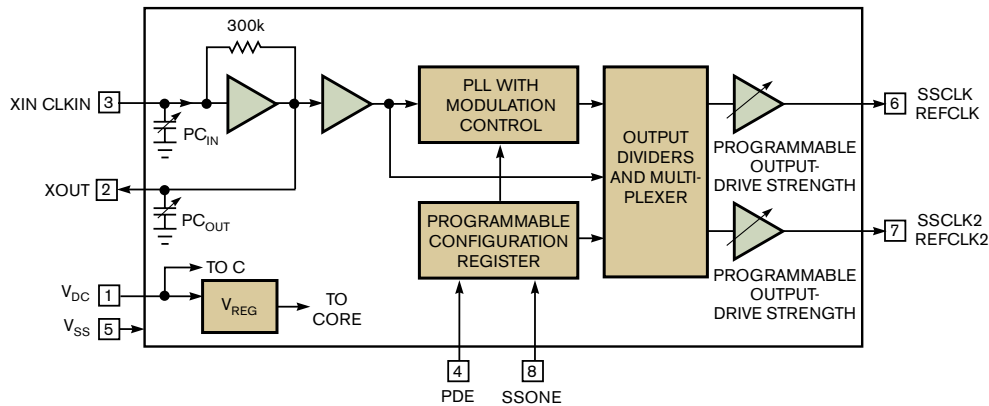


Figure 3 Users can dynamically update the SL15100 spread-spectrum-clock generator using the programmable configuration register.

same 66.666-MHz system clock with the same $\pm 1.5\%$ center spread and relative EMI reductions for the same harmonics using the triangular profile. The SSCG technique is analogous to the spread-spectrum technique in communications applications. However, it does not spread encoded information over a wide bandwidth, as CDMA (code-division multiple access) does, and the only benefit of using SSCG is to reduce undesired EMI emissions.

PROGRAMMABLE GENERATORS

The major advantage of using a programmable SSCG, such as the SpectraLinear (www.spectralinear.com) SL15100 (**Figure**

3), is that it improves and optimizes various timing specifications within the system-timing budget. One of the most critical considerations of clock-signal integrity is the matching of the impedance of the board trace and driven load to the clock driver. This matching ensures that the clock signal is free from overshooting or undershooting and ringing for each of the driven clock signals. Programmable clocks achieve this goal by providing adjustable impedance levels at each clock-output driver to ensure a good match to various load-impedance levels. Programmable-clock-drive-strength levels allow the user to match load-impedance levels at each output, to obtain matched impedance levels, and to optimize the signal integrity based on the actual levels the user measured during system evaluation. In addition, you can use the programmable-drive levels to control clock-signal rise and fall times within acceptable signal-integrity limits to slow the edges, which reduce high-frequency harmonic content and further reduce EMI. **Table 1** shows programmable parameters and ranges for the SL15100.

Frequency margining is the stepping up or down of output

frequency through frequency-control pins or the I²C (inter-integrated-circuit) interface. The technique is both useful and easy to implement under automated-testing systems to find potential system weaknesses and failures during the product-development and production phases. The fine, gradual increase or decrease of the system-clock frequency sweeps the range of the frequency to detect any irregularities or failures for a given frequency range, and you could easily implement it using programmable clocks by setting both center- and extreme-frequency limits for changing system requirements. In addition, you can test the margin of other critical timing parameters, such as clock skew, spread amplitude (percentage), or spread-modulation rates, to verify that the receiving PLL (phase-lock loop) in an ASIC or other system-component interface has sufficient built-in bandwidth and timing margins.

Programmable clocks are also beneficial during EMC (electromagnetic-compatibility) testing because you can easily set frequency modulation to any value from 0 to 5%. This programmable attribute of SSCG simplifies compatibility measurements during design and testing, eliminates product-introduction delays, and improves time to market. The second benefit of SSCG is reducing EMI without degrading the timing-signal quality. The system references setup-and-hold times to only the rising edge of the timing signal. Because the rise and fall time changes only by the amount of spread percentage when you use a spread-spectrum approach, the process maintains the critical setup-and-hold-timing margins.

Another benefit of using SSCG is that you can integrate additional programmable EMI-reduction and -timing functions into the same product, further enhancing system performance and reducing costs. Multiple-PLL and multioutput-SSCG products with selective use of spread-spectrum-clock functions enable users to integrate many functions, such as buffers and level translators. Using multiple unique programmable-frequency outputs in the same product eliminates a large number of crystals and crystal oscillators by using a single-standard, first-order crystal, saving additional cost and PCB space.

Even in systems meeting EMC requirements, SSCG could further reduce the emission levels to reduce the total number of PCB layers, leading to further cost reduction, as in low-cost consumer products, such as ink-jet or multifunction printers and PDAs.**EDN**

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1 Lexmark International, SSCG technology, US patents 5,488,627, 5,631,920, 5,867,524, 5,872,807, and 6,617,103.

AUTHOR'S BIOGRAPHY



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