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Simple toggle circuits illustrate low power-MOSFET leakage

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 The novelty circuit in **Figure 1** illustrates the extremely low gate-leakage current typical of modern power MOSFETs. You can find parts that, in a moderately dry environment, will hold their state for days at a time. In operation, if MOSFET Q_1 is off, the load—perhaps a lamp or a buzzer—pulls Q_1 's drain to

nearly the 12V-dc power-supply voltage. R_2 charges C_1 to practically the same voltage. If you tap momentary-contact switch S_1 , C_2 and the gate of Q_1 charge to about 99% of C_1 's initial voltage, assuming that the tap is short enough that C_1 doesn't discharge significantly back through R_2 to the drain of Q_1 , which is now at a low voltage. During the next couple of seconds, C_1 discharges through R_2 toward the new drain voltage of Q_1 , which now conducts current through load resistor R_1 .

In the construction of the circuit, you must ensure extremely low leakage from the MOSFET's gate node. You can omit C_2 if you use a switch with essentially no leakage, and you may find that the gate capacitance of Q_1 is enough and that the leakage is low enough that days pass before the output changes significantly. If you'd like to ensure a longer hold time, you

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can increase the value of C_2 . A modern polypropylene capacitor should have a self-discharge time constant measured in years if you keep it clean, dry, and not too far above room temperature. If you increase C_2 , proportionately increase C_1 and decrease R_2 to maintain an R_2C_1 time constant of about half a second.

Another curious behavior of this novelty circuit occurs if you hold down S_1 for a few seconds. The gate of Q_1 then goes to a voltage slightly higher than the gate's threshold voltage for Q_1 . If, for example, the power supply is 6V and the load is a 6V incandescent lamp and Q_1 's gate threshold is approximately 3V, the lamp will light dimly. When you release the switch, because a typical power MOSFET has a high rate of drain-current change with gate-voltage change—that is, transconductance—you can observe

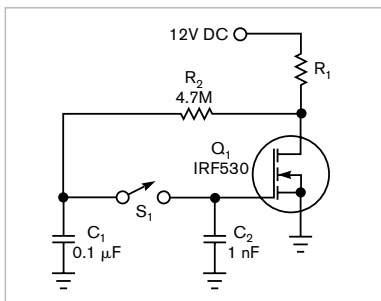


Figure 1 This “toggle” circuit demonstrates the low gate leakage of modern power MOSFETs.

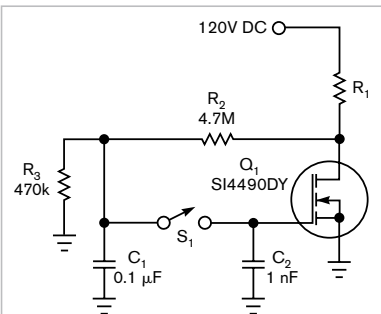
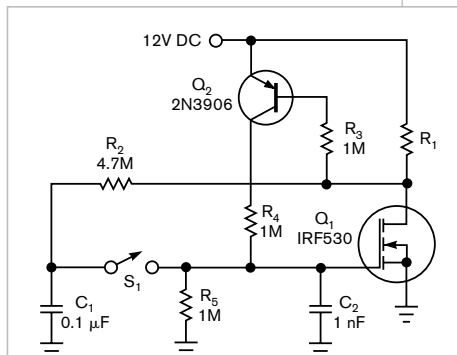


Figure 2 This circuit can control higher voltages because it supplements R_2 with a resistor to ground to form a voltage divider, ensuring that C_1 doesn't charge to a voltage that would destroy the gate of Q_1 .



NOTE: LOADS AS LARGE AS A FEW AMPS ARE POSSIBLE WITH THE RIGHT POWER MOSFET.

Figure 3 This version of the toggle circuit indefinitely holds a state.

the slow change in gate voltage as a change in lamp brightness. Any leakage is inside and external to Q_1 . You may be able to detect a change in lamp brightness within a few seconds. But, even if you don't notice it, some change of voltage will occur. If you tap S_1 several times at intervals of a few seconds, the lamp will soon toggle be-

tween full brightness and fully off.

To use the circuit to control higher voltages, you can supplement R_2 with a resistor to ground to form a voltage divider to ensure that C_1 doesn't charge to a voltage that would destroy the gate of Q_1 (Figure 2). For a more practical toggle circuit that will indefinitely hold a state, you can add a tran-

sistor and some resistors (Figure 3).

If Q_1 is on and powers the load, then Q_2 is also on, holding Q_1 's gate on at about half the power-supply voltage because of the voltage-divider action of R_4 and R_5 . Tapping S_1 toggles the output as before, and, with Q_1 off, Q_2 is also off, allowing R_3 to hold Q_1 's gate near ground potential. **EDN**

Circuit adds functions to a monostable multivibrator

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Gate generation is often an inevitable step in digital-signal processing. Invariably, the gate generation during event processing in a digital system uses the input trigger of a monostable multivibrator. The values of the RC (resistance-capacitance) components within the manufacturer-supplied parameters determine the gate

width of the output pulse of the monostable multivibrator. The monostable multivibrator generates only one-shots for each input trigger during event processing.

However, you can enhance the functional capability of gate generation of a monostable multivibrator with modifications in its input-trigger circuitry

to generate any number of output-gate pulses for each single-input triggering. You can exploit the resultant circuit to generate a fixed number of repetitive gate pulses with a single-input trigger by incorporating a counter with the circuit to keep track of the gate generation. The monostable multivibrator becomes inactive as soon as it generates the requisite number of gates.

Figure 1 shows modifications to a monostable multivibrator that allow it to repetitively generate 63 gate pulses with one trigger. The RC components determine a gate width of 5 to 75 μsec . However, this design has a preset gate width of 20 μsec to give a total time

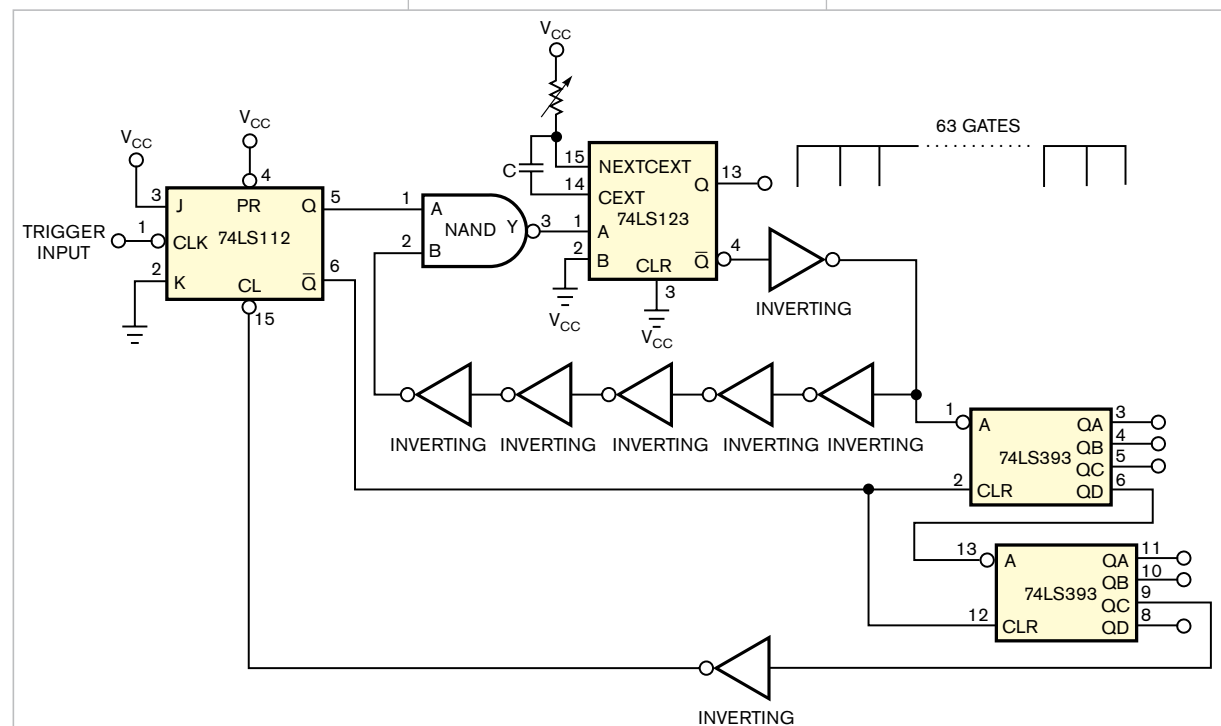


Figure 1 By adding counters and an oscillator to the output of a monostable multivibrator, you can generate any number of output-gate pulses.

interval of 1260 μ sec. When the input-trigger pulse goes to the active low, Pin 1, of the JK 74LS112 flip-flop, the falling edge of the input-trigger pulse activates the flip-flop to set Q. Because the default condition of Pin 2 of the NAND gate is at a high level, the transition at the output pin, Pin 3, of the NAND gate passes on to the active-low input of the monostable multivibrator at Pin 1. The falling edge of the output pulse of the NAND gate triggers the monostable multivibrator to generate the first gate pulse of predefined gate width.

Subsequently, when the Q output pulse of the monostable multivibrator makes a transition from high to low, the rising edge of the complementary output pulse of the monostable multi-

vibrator at \bar{Q} , Pin 4, connects back to the two-input NAND gate. Through a series of inverter retriggers, the monostable multivibrator again generates the next gate pulse. The gate generation can continue indefinitely. However, the \bar{Q} output after inversion also feeds into two 74LS393 hex counters. The two hex counters cascade together to count the 63 gate pulses. As soon as the circuit counts the requisite number of gate pulses, Pin 9 of the hex counter goes high and, after inversion, clears the active state of the JK flip-flop.

The two-input NAND gate's Pin 1 also goes to a low level and disables the flip-flop, preventing the feedback rising-edge transition of the \bar{Q} of the monostable multivibrator from again passing on to the trigger input—Pin 1 of


the monostable multivibrator. So, the trigger to the monostable multivibrator and further gate generation stop (references 1 and 2).EDN

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Piezoelectric driver finds buzzer's resonant frequency

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 Piezoelectric buzzers find wide use as audible-signal generators because of their low power consumption and clear, penetrating sound. An external driver or a self-driven circuit that oscillates at the resonant frequency of the piezoelectric element can drive these buzzers. A piezoelectric element produces the maximum

sound output at its resonant frequency. However, the resonant frequency of a piezoelectric element can have a tolerance as great as $\pm 15\%$. An external driver tuned to the nominal resonant frequency is therefore likely to miss the actual resonance point. This Design Idea externally drives a piezoelectric element and automatically

finds its actual resonant frequency.

The basis for operation is the following principle: When you apply an alternating voltage to the terminals of a piezoelectric element, the element will begin to vibrate. If you remove the excitation, vibrations will continue in a damped manner before they cease altogether. These residual vibrations will cause damped oscillations at the terminals of the piezoelectric element. If the excitation is close to the resonant frequency, the vibrations will be stronger and the residual oscillations will last

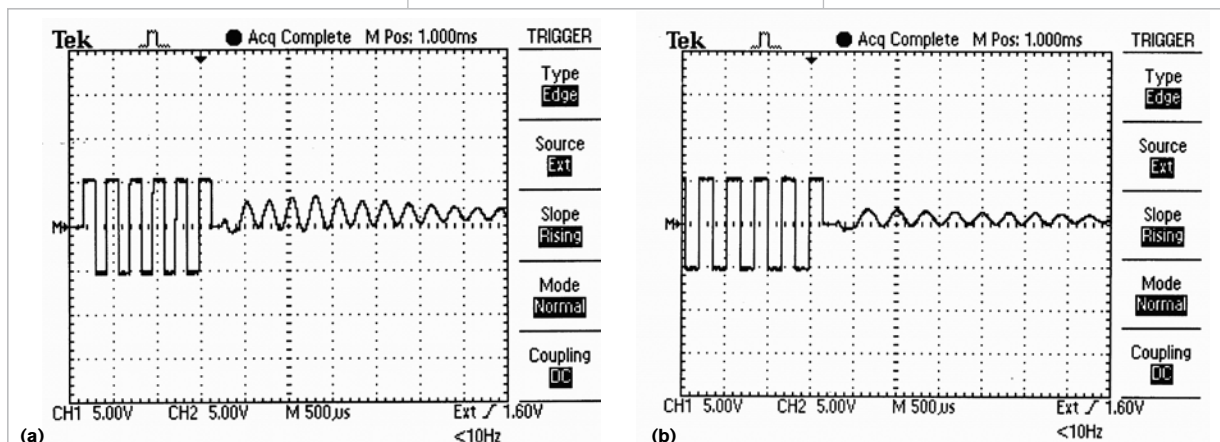


Figure 1 At a frequency of 4 kHz, which is closer to the resonant frequency, residual oscillations last longer (a) than the resonant frequency with 3.2 kHz (b).

longer (Figure 1). You can determine the actual resonant frequency by trying all the frequencies around the nominal resonant frequency and comparing the duration of residual oscillations.

In this design, a Microchip (www.microchip.com) PIC18F452 microcontroller drives a piezoelectric element through its I/O pins, RB4 and RB3 (Figure 2). Initially setting RB3 to zero and RB4 to one and toggling them after each half-period generates an alternating piezoelectric voltage (V_p) with a 0V-dc bias. After applying 10 cycles, RB3 is kept low, and

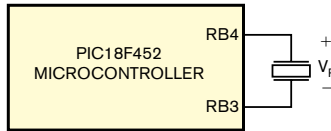


Figure 2 A PIC18F452 microcontroller first drives the piezoelectric buzzer at a programmed frequency and then configures one of its pins as an input to count the residual oscillations.

RB4 is made an input to count the low-to-high and high-to-low transitions of

V_p . Enabling the “interrupt-on-port-change” feature of Port B for 10 msec and incrementing a counter in the interrupt-service routine counts the transition of the piezoelectric voltage. Listing 1, which is available in the Web version of this Design Idea at www.edn.com/080807di1, demonstrates this feature. The program repeats these steps for all frequencies of interest and identifies the frequency corresponding to the maximum number of transitions at the resonant frequency. You can easily expand the idea for the case of multiple resonant frequencies.EDN

Low-cost digital DAC provides digital three-phase-waveform synthesis

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Many applications involve the digital synthesis of three-phase sinusoidal waveforms, such as ac-motor drives, active power filters, and grid-voltage synchronizers, that use a mi-

crocontroller or a DSP for digital control. You can perform this synthesis by using conventional analog techniques (Reference 1) or DDS (direct digital synthesis). Digital techniques provide

higher stability and the ability to incorporate frequency, phase, and amplitude adjustments. For applications requiring 16-bit or higher-resolution, three-phase-signal synthesis, DDS involves the use of a microprocessor or a DSP to interface multiple DACs. This approach uses not only a lot of devices, but also supporting components and board space. Although one device can have multiple-output serial-controlled DACs with four, eight, 32, or more

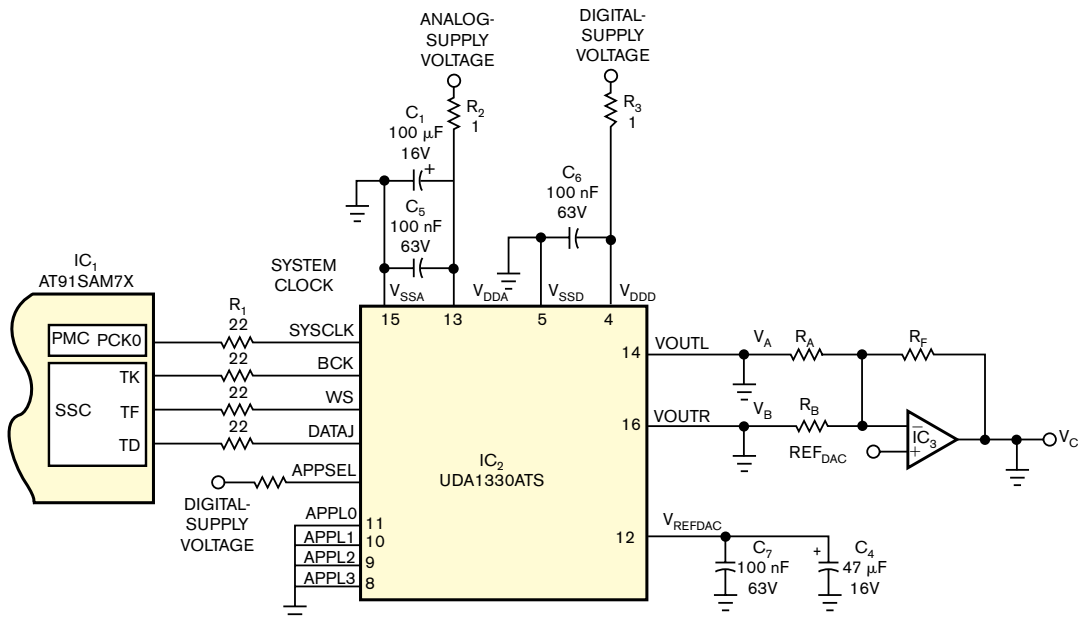


Figure 1 This scheme implements three-phase DDS (direct digital synthesis) with few components. The code in the ARM processor provides the ability to incorporate arbitrary frequency, phase, and amplitude adjustments with 16-, 18-, or 20-bit resolution.

channels, the DACs provide few bits at the expense of the number of channels. Hence, using multiple-output DACs is an unappealing approach.

Alternatively, you can use shift registers or switched-capacitor filters, but this approach also involves a high parts count, and the lack of phase and amplitude adjustment makes this method inappropriate for high-resolution DDS (**Reference 2**).

In contrast, stereo DACs are readily available. Their widespread use has produced low-cost, high-quality components. For example, the NXP UDA1330ATS has an I²S-serial data-format interface; word lengths of 16, 18, and 20 bits; and sampling frequencies of 8 to 55 kHz (**Reference 3**). These features make the DACs attractive for three-phase DDS with few components.

This Design Idea implements DDS techniques using an ARM microcon-

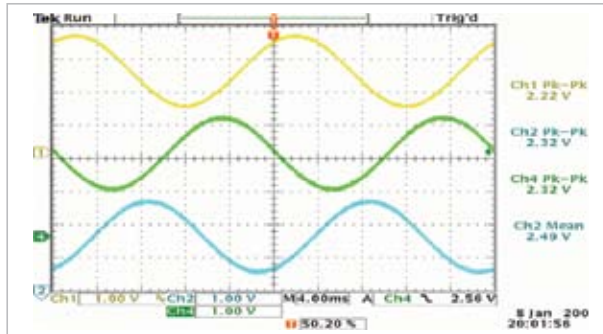


Figure 2 Traces 1 and 2 show the voltage outputs from the DAC. Trace 4 is the third channel that an inverting, summing op amp provides.

troller, IC₁; one stereo-DAC, IC₂; and one op amp, IC₃ (**Figure 1**). The ARM AT91SAM7X256 code in **Listing 1**, available in the Web version of this Design Idea at www.edn.com/080807di2, generates a table containing the cosine function of the desired resolution and length. The table produces $\cos(\alpha + 2/3\pi)$ and $\cos(\alpha - 2/3\pi)$. The ARM microcontroller sends the data using I²S-serial format by using interrupts attaching the ISR (interrupt-service rou-

tine) whenever the output buffer is empty. **Listing 2**, also in the Web version of this article, shows how to achieve an ISR to send the data. IC₂ provides voltage outputs V_A and V_B , which are two of the three signals for a maximum amplitude of 5V p-p, but with an offset of 2.5V. You can derive the third channel as a function of the other channels. You can easily implement this operation using a single inverting, summing op amp, IC₃, and the 2.5V DAC reference for canceling the offset. In this case, $R_F = R_A = R_B = 10\text{ k}\Omega$ for obtaining unity gain, and you could add a potentiometer in the inverting pin for an exact offset cancellation if the resistors don't match exactly.

Figure 2 shows the synthesis of the three-phase waveforms. For further explanation and to access the **references** to this article, go to www.edn.com/080807di2. **EDN**