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AND FRAN GRANVILLE

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Astable multivibrator lights LED from a single cell

Luca Bruno, ITIS Hensemberger, Monza, Lissone, Italy

Lighting LEDs from a single 1.5V cell poses a problem because their forward voltages are higher than the cell's. The simplest way to light the LED is to use a step-up dc/dc converter. This Design Idea offers a simple and reliable alternative for applications in which low cost is of primary concern. The circuit in **Figure 1** employs a classic astable oscillator, which transistors Q_1 and Q_2 form. The square-wave drive signal at Q_2's collector turns a PNP switching transistor, Q_3, on and off. When Q_3 turns on, it charges inductor L_1, and, when it turns off, inductor L_1 discharges its stored energy through the LED during flyback, allowing you to light any type or color of LED.

The astable circuit oscillates at a frequency of $1/T_O$, where $T_O=T_L+T_H$ with $T_L\simeq0.76R_2C_2$ and $T_H\simeq0.76R_1C_1$ when the cell voltage is 1.5V, where T_O is the time, T_L is the on-time, and T_H is the off-time. With the component values in **Figure 1**, the frequency and the duty cycle are about 28.5 kHz and 50%, respectively. During the on-time, transistor Q_3 is on, and inductor L_1 starts to charge with constant voltage so its current ramps up linearly to a peak value, as the following **equation** describes: $I_{L1PEAK}=[(V_{BAT}-V_{CESATQ3})/L_1]\times T_L$, where I_{L1PEAK} is the peak current of L_1, V_{BAT} is the battery voltage, and $V_{CESATQ3}$ is the collector-to-emitter saturation voltage of Q_3. During the off-time, Q_3 is off, and the inductor's voltage reverses polarity, forward-biasing the LED and discharging through it at a constant voltage roughly equal to the forward voltage of the LED while its current ramps down to zero.

Because this cycle repeats at a high rate, the LED appears always on. The LED's brightness depends on its own average current, which is proportional to the peak value. Because the LED current is roughly a triangular pulse with a peak current approximately equal to the inductor's current because of the finite turn-off time of Q_3, you can easily estimate the average current: $I_{LEDAVG}\simeq(\frac{1}{2})\times I_{L1PEAK}\times(T_{DIS}/T_O)$, where T_{DIS} is the discharge time of inductor L_1 through the LED, which you can roughly estimate from the slope of L_1's discharge, which is V_{LED}/L_1, where V_{LED} is the LED's voltage.

To control the LED's brightness, you may increase or decrease the inductor's peak current by varying its inductance from 100 to 330 µH to achieve the optimal brightness for the type of LED you are using. However, L_1's charge slope is always smaller than its discharge slope, and, because T_L and T_H are equal, L_1 has enough time to discharge completely. When it recharges on its next cycle, its current

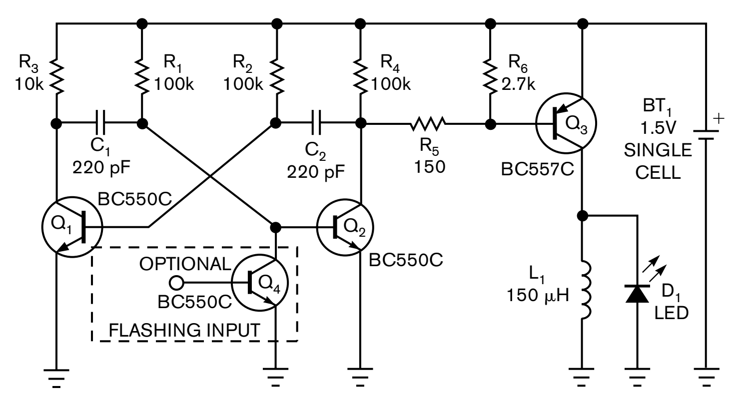

Figure 1 This simple astable multivibrator provides a low-cost way to drive an LED from a single cell.

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cycle always starts from zero. If this is not the case—if you reduce T_H too much, for example—the inductor current increases on each cycle until Q_3 goes out of saturation, and the final current value becomes unpredictable because it depends on Q_3's dc gain. Optional transistor Q_4 allows the circuit to flash the LED when a low-frequency gating signal drives its base.

No one component is critical; for example, any small-signal transistor is suitable. But, if possible, choose a PNP transistor for Q_3 with high dc-current gain and low collector-to-emitter saturation voltage for best efficiency. Also, take care that the peak current does not saturate L_1 and does not exceed the maximum peak-current rating of Q_3 and the LED. The astable circuit starts to operate with a supply voltage as low as 0.6V, but the LED is off and begins to light dimly when the supply voltage exceeds 0.9V. When the supply voltage exceeds 1V, the LED's brightness is adequate, even if it depends slightly on the forward voltage of the LED. **EDN**

IC provides versatile toggle functions

Louis Vlemincq,
Belgacom, Evere, Belgium

The circuit in **Figure 1** offers not only as many as six channels in a single IC package, but also a high level of additional flexibility. The configuration of Output 1 is a "plain-vanilla" toggle. A resistive divider comprising R_1 and R_2 provides a midsupply bias to all the channels through resistors R_3, R_6, R_7, R_{10}, and R_{12}. Because the bias voltage of R_1/R_2 is within the hysteresis range of the gates, they behave as flip-flops, retaining their high or low state in a stable manner.

Debouncing capacitors C_2, C_3, C_4, and C_5 charge to the level of the output. Pushing switch S_1 inverts the output state because of the inverting action of the gate. This state remains stable because, in the first gate's circuit, for example, R_4's value is larger than that of R_3, and R_4 cannot overcome the hysteresis threshold of the gate. Only the discharge of C_2 can accomplish that task. When you release the pushbutton, C_2 fully charges after the debouncing delay, and the circuit is ready for another inversion. C_1 provides a general power-on-reset feature to all the channels. If your circuit requires only one channel, you can directly connect R_1 and R_2 to the input of the gate, omitting R_3.

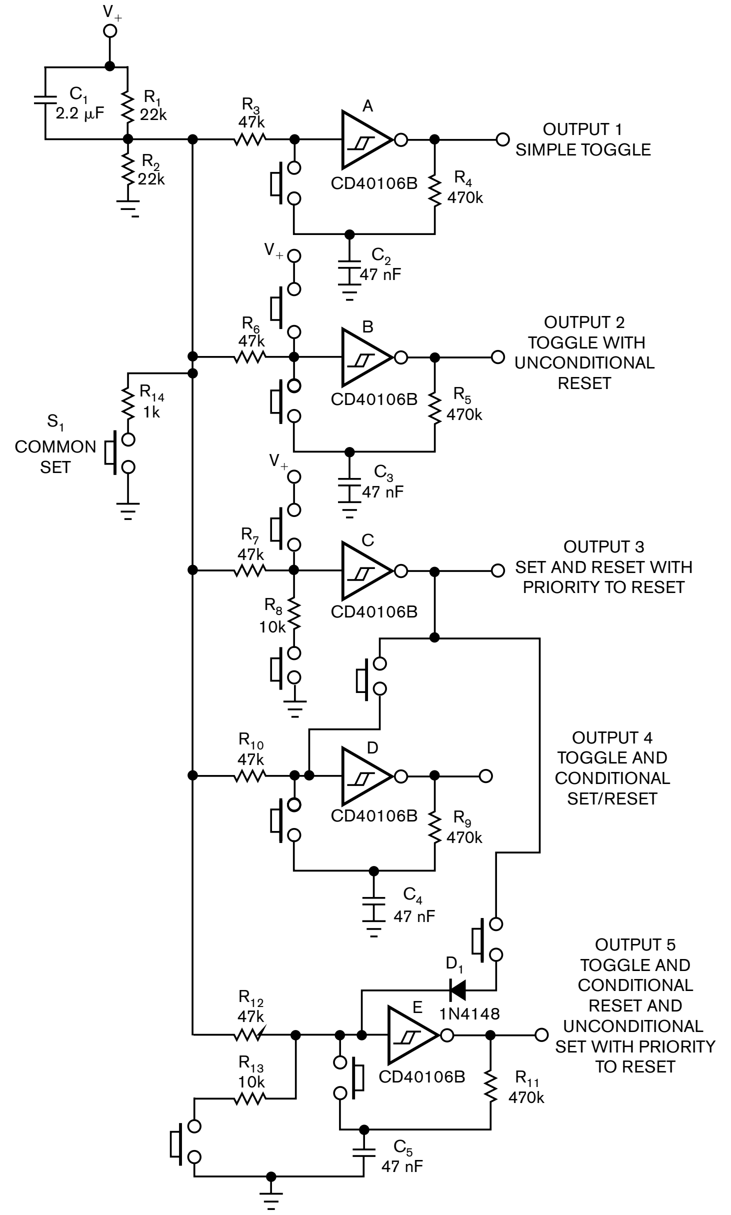


Figure 1 This circuit shows multiple Schmitt-trigger inverters functioning as a variety of set/reset toggles.

Output 2 has the same toggle function as Output 1 but also includes a direct reset. Output 3 works only in a set/reset mode; the position of R_8 determines the priority state. Output 4 also has a toggle action, but you can set or reset it to a state opposite that of Output 3. Output 5 works in a similar manner, except it allows only a conditional reset because of the position of D_1. Output 5 also includes a forced, nonpriority set. You can mix and match all these functions, providing almost unlimited versatility.

The IC in **Figure 1** is a Fairchild Semiconductor (www.fairchildsemi.com) CD4000-series circuit, suitable for supplies of 3 to 15V, but it could also be a 74AC14 or 74HC14 from NXP (www.nxp.com), for example. Any CMOS-input gate having a Schmitt-trigger action is suitable. You must take care to bias the inputs in the middle of their hysteresis range. HCMOS circuits would require an average bias of approximately 1.2V for a 5V supply, for example.**EDN**

Instrumentation amp has low offset, drift, and low-frequency noise

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Analog Devices' (www.analog.com) digitally gain-programmable AD8231 instrumentation amplifier exhibits zero offset. It has programmable voltage gains, which are successive powers of two, from $2^0=1$ to $2^7=128$ (**references 1** and **2**). The AD825x family also includes some digitally gain-programmable instrumentation amplifiers, which have gain expressed as powers of 10. These amplifiers contain no internal autozero circuitry, however. The composite instrumentation amplifier in **Figure 1** suits applications requiring instrumentation amplifiers having voltage gains of a multiple of 10 and requiring low voltage offset, drift, and low-frequency noise.

The design exploits the fact that the gain is 10^M, where M is an integer, which you can express as $10^M=2^M\times5^M$. The circuit in **Figure 1** employs a cascade of the autozeroed AD8231 instrumentation amp, IC_1, with a preset voltage gain of eight, IC_2, and IC_3. The net result is that the input-voltage offset of IC_2 causes an RTI (referred-to-input) voltage offset, which decreases by a factor of eight compared with an offset of a stand-alone circuit, IC_2. The same holds also for the offset-voltage drift. The auto-zeroing circuitry of the IC_1 decimates the low-frequency noise.**EDN**

REFERENCES

1 "Zero Drift, Digitally Programmable Instrumentation Amplifier, AD8231," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8231,00.html.

2 "10 MHz, 20V/s, G=1, 2, 5, 10 iCMOSR Programmable Gain Instrumentation Amplifier, AD8250," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8250,00.html.

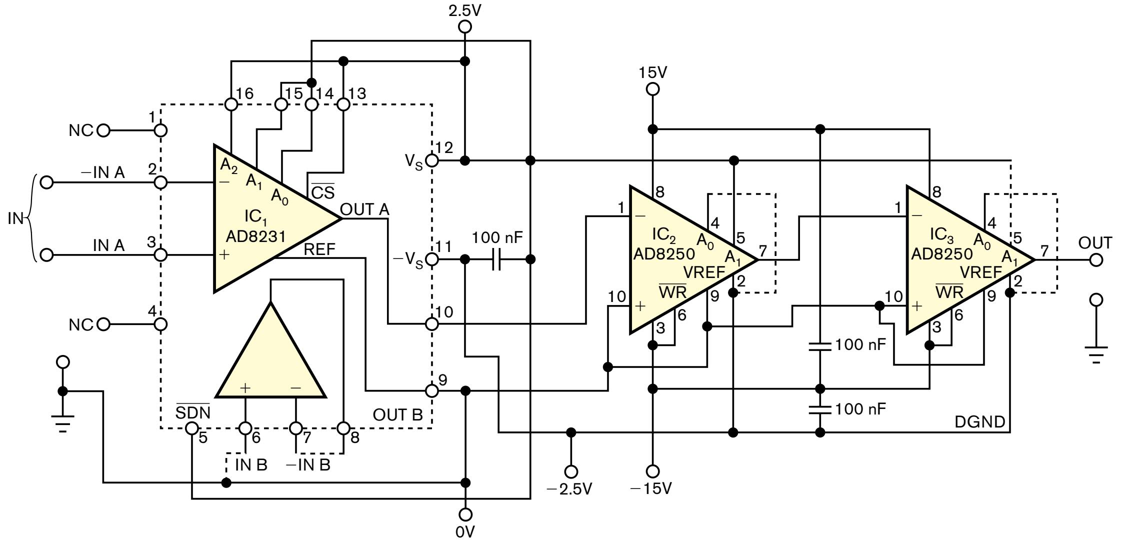


Figure 1 By cascading an autozeroed instrumentation amplifier having a gain of 2^3 and instrumentation amplifiers having gains of five, you get a decade-gain instrumentation amp whose dc performance is much better than that of monolithic decade-gain instrumentation amps.

Four DIPs provide as many as 80 sequential-LED outputs

Greg Carkner, Cobourg, ON, Canada

A previous Design Idea makes clever use of the ability of the 4017 CMOS counters to accept either positive or negative edge-clock signals, even though it leaves two LEDs on at once (**Reference 1**). But what happens if you want more than 19 counts? A quick check in some old CMOS data books uncovered a circuit for using 4017 counters to make sequential displays. However, this approach sacrifices some outputs and yields nine outputs for the first counter and only eight for each subsequent one. It also requires you to add an AND gate between each successive counter stage.

The circuit in **Figure 1** differs from the one in the earlier Design Idea in that it uses HCMOS parts and adds one 74HC540 to facilitate a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs. The 74HC540 is a convenient pinout version of the venerable 74HC240-series bus drivers. By including a DIP-resistor network, you can also reduce the discrete-component count for the design. The recommended current-sourcing capability of the HC-series parts at 6V supply is slightly lower than that of the 4000-series parts at 15V, but the reduced resistor losses provide a more energy-efficient circuit if you use better LEDs.

The **figure** omits the necessary supply-bypassing capacitors or a clock or power-on-reset circuit. D_1, D_2, and R_1 form a simple AND gate, which you might use instead of an external reset input to form a continuous ring counter, at which the cathodes connect to selected outputs of each of the counters, IC_1 and IC_2. **EDN**

REFERENCE

1 Tregre, Jeff, "Cascade two decade counters to obtain 19 sequential outputs," *EDN*, Dec 14, 2007, pg 62, www.edn.com/article/CA6512153.

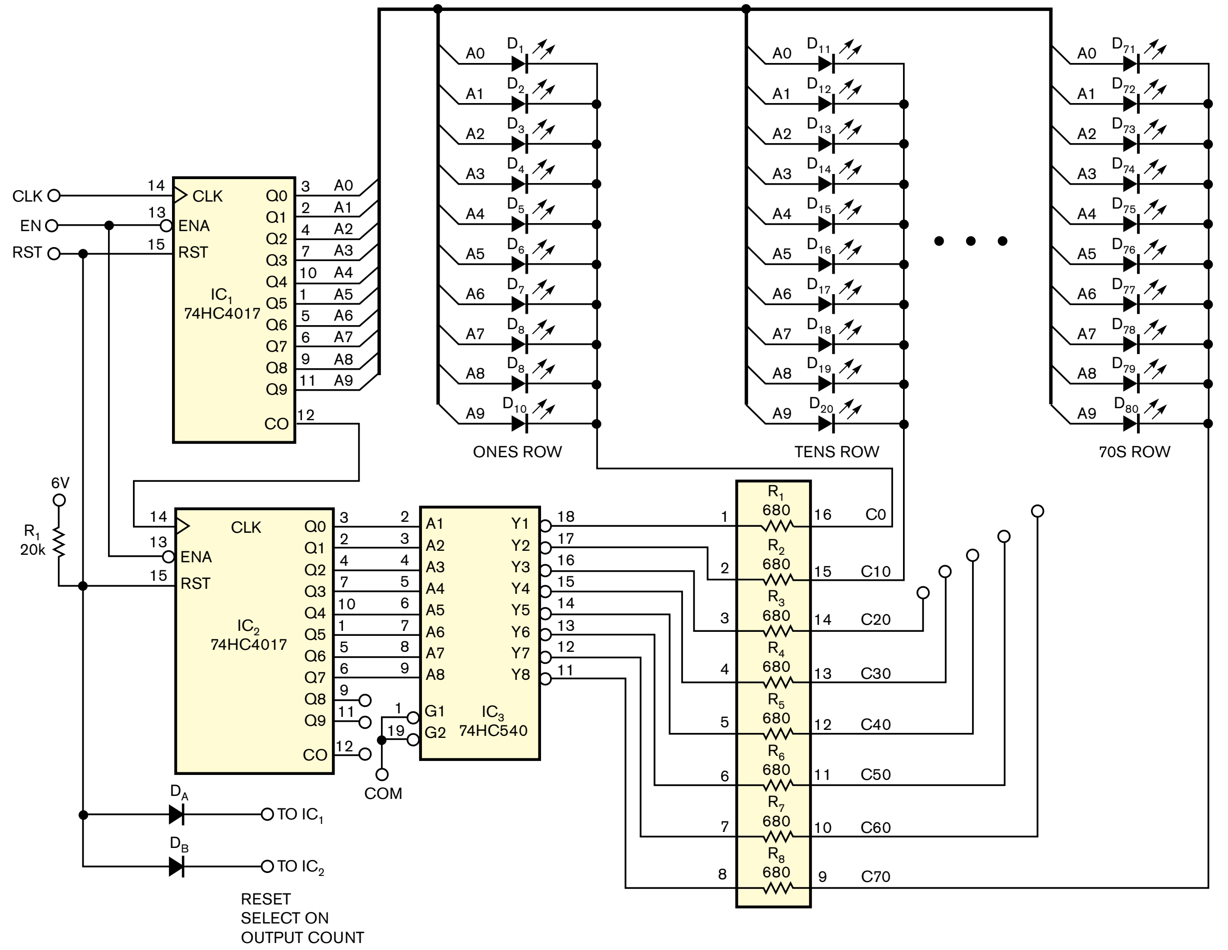


Figure 1 This circuit provides a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs.

Program an op-amp gain block with a limited-adjustability, monolithic, solid-state resistor

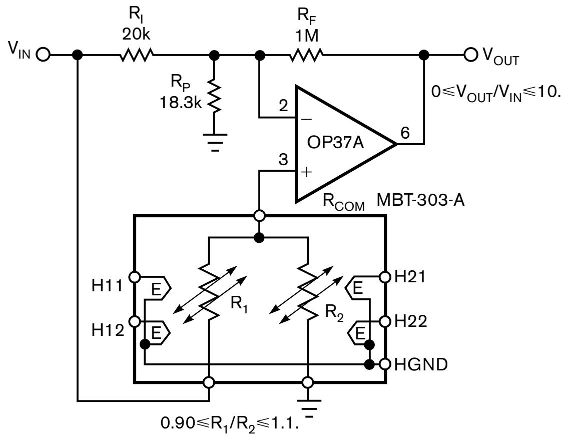
W Stephen Woodward, Chapel Hill, NC

Solid-state replacements for traditional electromechanical trimmer potentiometers are increasingly available in a variety of technologies from a variety of vendors. These replacements have many obvious advantages, such as automatic adjustability, miniaturization, and immunity to vibration. Some of these devices have only limited programmable spans, however. This limitation can sometimes be problematic and may preclude the use of a solid-state option in some design applications. An example of this shortcoming is the Rejustor family of devices, which Microbridge (www.mbridgetech.com) recently introduced. The MBT-303-A Rejustor voltage divider is programmable over a span of only ±10%. When such a limited-capability device sets the gain of a typical amplifier circuit, the correspondingly narrow range of accessible gains may be woefully inadequate.

Figure 1 suggests a generally applicable workaround that works not only with rejustors, but also with all limited-adjustability, programmable dividers with a ±10%-ratio-adjustment range. It uses a single op amp in a differential topology that, in effect, subtracts the minimum programmable-divider ratio from the maximum and amplifies the difference. This approach expands the programmable-gain span to include zero and any desired figure. Potential applications for this trick include any design situation requiring a wide range of inverting and noninverting programmable-gain factors.

Although the circuit in **Figure 1** implements a programmable gain of zero to 10, you can implement almost any range with a suitable choice of resistors and op amps. **Figure 2** illustrates a gain of zero to −10 for the inverting case. The design equations are R_F/R_I, which is five times the maximum desired gain; $R_P=1/((1/0.9/R_I)-(1/R_F))$ for noninverting gain; and $R_P=1/((1/1.1/R_I)-(1/R_F))$ for inverting gain. The availability of stock resistances sometimes determines a starting value for R_I or R_F. For example, the circuit in **Figure 1**, where R_F has a value of 1 MΩ, accommodates the fact that many inexpensive precision-resistor families, such as those made of metal film, have maximum resistances of 1 MΩ. However, if resistor availability isn't a factor, then choosing R_I to have the same value as R_1 minimizes sensitivity to op-amp bias-current errors. Choosing R_P midway between the resistances for the noninverting- and inverting-gain equations reveals an additional flexibility of the circuit. That variation results in a bipolar—that is, both inverting and noninverting—gain range, with a gain of zero at midspan.

This topology eliminates the inflexibility penalty that limited divider programmability imposes. This benefit, however, incurs a price in the op amp's performance. Because of the partial cancellation of amplifier gain, the gain-bandwidth product and dc accuracy of the op amp must surpass the overall maximum gain and offset requirements of the gain block by at least a factor of five. One way to accommodate this requirement is to incorporate a decompensated, precision op amp, such as the classic OP37, which is stable only for closed-loop gains higher than five. **EDN**

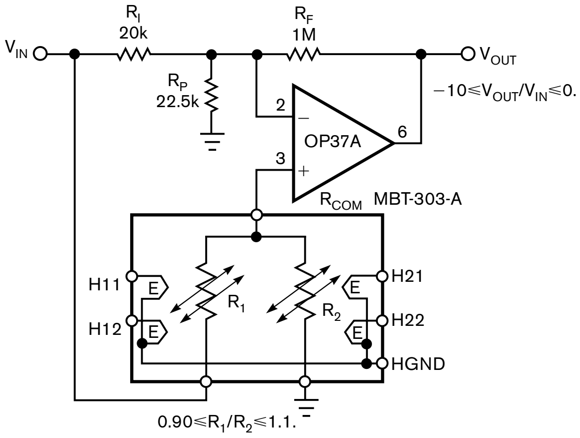


NOTES:

Set R_P=20.4 kΩ FOR A PROGRAMMABLE-GAIN RANGE OF $-5\le$GAIN$\le+5$.

$V_{OUT}/V_{IN}=50(R_2/R_1-0.9)=0$ IF $R_2/R_1=0.9$ AND $=10$ IF $R_2/R_1=1.1$.

Figure 1 Adding an op amp and associated components to a Rejustor solid-state resistor allows you to trim the output over the full input-voltage range.



NOTE:

$V_{OUT}/V_{IN}=50(R_2/R_1-1.1)=0$ IF $R_2/R_1=1.1$ AND
$=-10$ IF $R_2/R_1=0.9$.

Figure 2 Adjusting the value of R_P allows the circuit to function as an inverting trimmer.