

On-chip test capabilities solve the analog-test problem for high-speed serial interfaces

INCLUDING ANALOG-TEST HARDWARE IN AN SOC PROVIDES VISIBILITY INTO THE PERFORMANCE OF ON-CHIP SERIAL LINKS, HELPING TO ENSURE SIGNAL INTEGRITY AND REDUCE THE COST OF MANUFACTURING TEST.

A small amount of on-chip analog-test hardware offers big payoffs when you are dealing with high-speed serial interfaces. As part of the serial-interface IP (intellectual property) or of an IP wrapper, the test hardware can provide views of the interface's performance that are more accurate than those of expensive external test equipment. As high-speed serial interfaces increase in speed, on-chip diagnostics will be the only way to verify that serial links—particularly the PHY (physical) interface—are working correctly at the designated speed.

Even today, interfaces such as PCIe (peripheral-component-interconnect express), SATA (serial advanced-technology attachment), and XAUI (10-Gbps attachment-unit interface) greatly benefit from the use of on-chip diagnostics to support rates of 2.5, 3, and 3.125G transitions/sec, respectively. Internal diagnostics enable a designer to observe the received eye diagrams and perform signal-integrity analysis of the link. Visibility into the on-chip signal is useful with PHY interfaces that have tunable equalization. If the point of visibility comes after any front-end equalizers in the receiver, a designer can directly observe the effects of receiver equalization. The effects of equalization are visible from transmitter to receiver.

Additionally, the on-chip diagnostics permit at-speed, mixed-signal tests during production test with low-cost digital testers, thereby eliminating the need for expensive analog-test equipment. With the right configuration, these diagnostics can reduce analog tests to a simple digital scan.

SOC-SERIAL-INTERFACE-TEST ISSUES

Serial links eliminate setup-and-hold requirements on data lines, require fewer I/O pins, and are higher performance than parallel links. These advantages come with trade-offs. For example, you must run careful signal-integrity analysis of the SOC (system-on-chip) package and PCB (printed-circuit-board) layout to minimize return loss and crosstalk. Additionally, debugging is more difficult because a standard logic analyzer cannot easily connect to a high-speed serial link. So, debugging signal-integrity issues requires expensive test equipment, such as a multigigahertz oscilloscope or a VNA (vector-network analyzer).

As serial rates increase to 5G, 6G, and even 10G transitions/sec for PCIe 2.0, SATA, and IEEE 802.3ap, respectively, bond

wires in an SOC package represent a significant portion of the signal wavelength. PCB vias become more disruptive, and connectors cause more problems due to impedance mismatches. Crosstalk increases, and jitter becomes a big concern. In addition, insertion loss across a PCB backplane becomes steadily greater with frequency (**Figure 1**). Without receiver equalization and transmit pre-emphasis, the received eye can remain closed for many of these links, as an animated demonstration that you can find in the Web version of this article at www.edn.com/ms4285 dramatically shows.

For these reasons, the PCIe standard has gone through a significant evolution to make 5G transitions/sec workable. For example, board traces must be 85Ω rather than 100Ω to maximize trace lengths, and the standard calls for two transmitter-equalizer settings plus two autonegotiated speeds. Although the original 2.5G-transitions/sec PCIe interface required interoperability simulations only for calculating channel losses with a 13.2-dB maximum, the 5G-transitions/sec version requires the use of measured S parameters. Designers then use these parameters to calculate insertion loss, return loss, and crosstalk in time-based

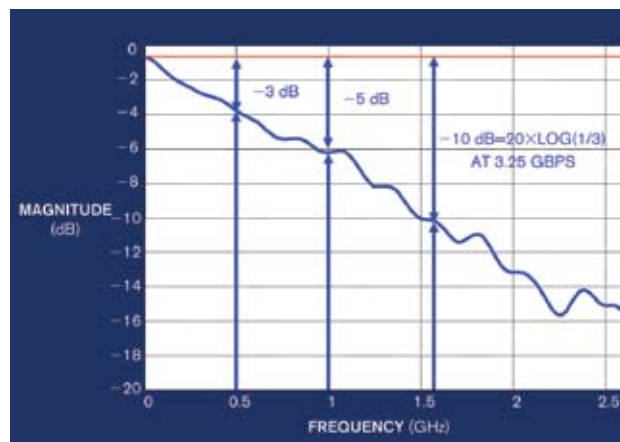


Figure 1 Off-chip factors limit the ability to measure a high-speed serial link's performance, as the insertion loss across 34 in. of FR4 PCB indicates. This loss curve was measured using a pulse-response technique that produces results similar to those you can obtain with a vector-network analyzer. The bounces indicate reflections or impedance discontinuities in the channel.

simulations. The transmitter must meet these specifications for the output and across the channel.

A simulation, even one you base on measured S parameters, is one thing. But, with the PCB-related issues of 5G- or even 2.5G-transitions/sec signals, how can a designer be sure he is receiving accurate information about a serial link's performance in an actual chip without looking at the entire channel of the silicon's transmitter-output-to-receiver input? Integrating test capabilities into the chip is the only way to avoid the distortions that may affect off-chip measurements and to see what the receiver is seeing.

TEST STRATEGY

It is crucial to recognize that emerging serial links are changing the rules for dealing with high-speed data-transfer devices. Simple loop-back tests cannot reliably provide on-chip performance for links that run at speeds greater than 3G transitions/sec. Errors simply may not be measurable, in part because the SOC environment differs from that of the traditional PCB environment, which also contributes to measurement uncertainty. As University of California—Los Angeles professor Ken Yang points out, SOCs experience system-interaction-induced errors from variables such as packaging, temperature, and voltage, all of whose effects are invisible outside the chip. At sufficiently high speeds, SOCs containing serial links become untestable using traditional external testers.

A typical test suite to judge the performance of a PHY interface in a high-speed serial interface includes tests of BER (bit-error rate), asynchronous BER, transmitting voltage, eye mask, transmitter jitter, receiver offset, and received voltage level. Most of these tests rely on analog-signal measurements that an

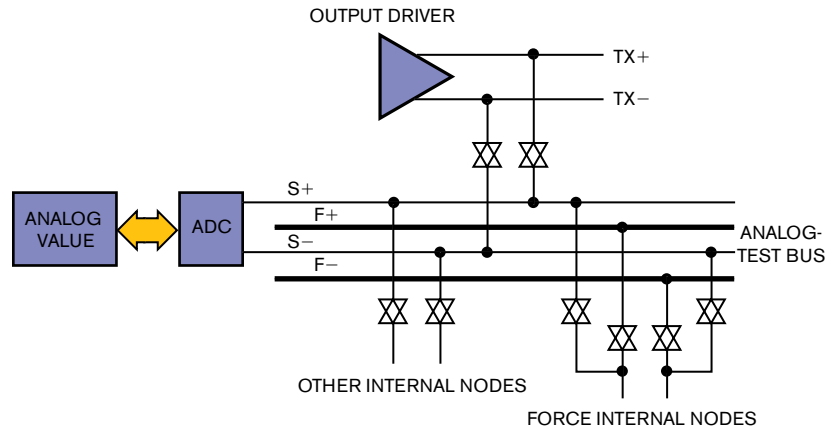


Figure 2 An on-chip analog-test bus connects to an ADC to provide the basis for complete visibility to the performance of high-speed serial links. Similar to standard scan methodologies, the analog-test bus enables scan-in of test vectors and scan-out of digitized analog values, as well as pass/fail indications from compare registers.

ADC can capture. Because the objective is to eliminate the possibility of signal distortions from the chip's package and other parts of the I/O channel, the chip must integrate the ADC.

Standard digital-scan methods provide a good model for creating this visibility into the on-chip performance. For digital-circuitry testing, control circuitry loads serial-scan data into registers and then scans the combinatorial results from the registers. Software tools offer comprehensive support for digital-scan methodologies, including providing help in developing test patterns and measuring test coverage. With an area overhead of less than 15% for the average chip, scan methods provide observability of internal digital signals and enable simple automated testing.

To get this same level of internal testability for analog cir-

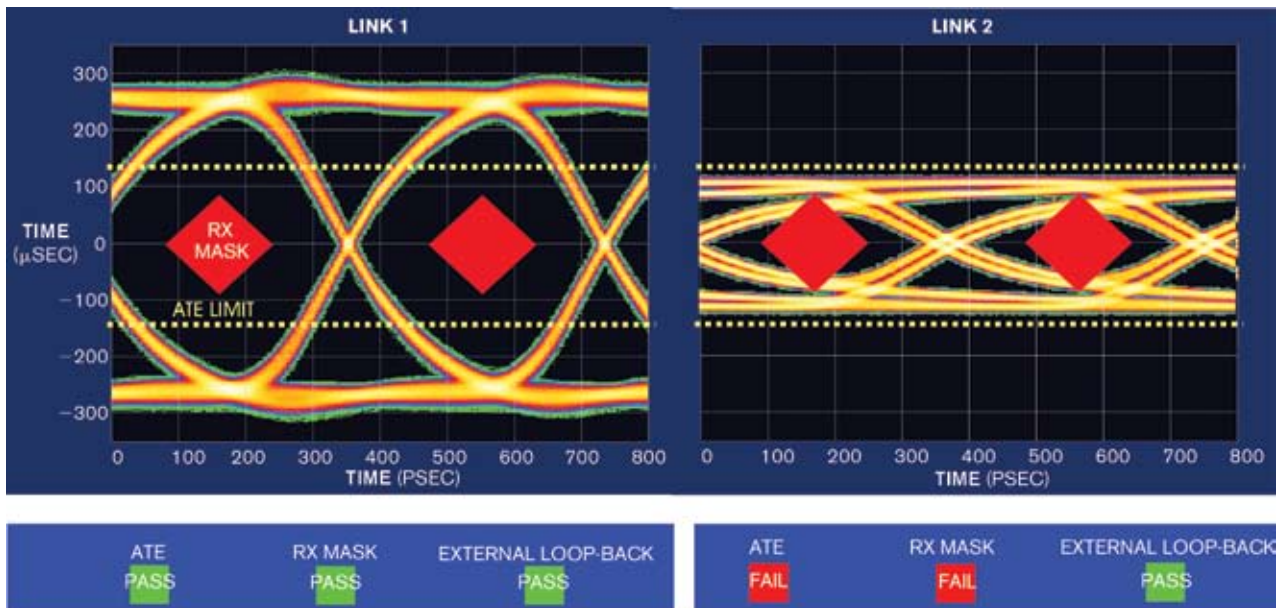


Figure 3 Traditional loop-back tests, such as this one on a PCIe eye mask, often fail to give accurate results when link speeds increase into the multiple-gigatransitions/sec range.

cuitry, you must include some type of analog-test bus. **Figure 2** shows a straightforward analog bus that has four interconnect wires: two force lines and two sense lines. An associated four-pin JTAG interface can handle all setup and measurement tasks. Once the bus is in place, you can integrate additional resources around the analog-test bus, enabling a versatile set of built-in analog-test capabilities that can fully test the performance of a PHY interface. With resources on-chip, all external access to the PHY interface can be through a simple digital port. As the next section explains, it is possible to reduce all analog-test results to a single pass/fail bit. Using this approach, you can reduce a complete analog-test approach to the process of accessing a simple digital interface, such as JTAG, with no external analog equipment.

CONVERTING ANALOG TESTS TO DIGITAL

Measuring an analog value, such as transmitting amplitude using an on-chip ADC, results in a continuous range of acceptable and unacceptable values and, in turn, a true analog result. Once you convert this result to a digital value, a tester could read the result and convert it into a pass/fail result within a set of acceptable limits. However, this type of pass/fail testing requires someone to write a test program to read the value, convert the value, compare it with acceptable limits, and determine pass or fail requirements. Someone must also debug and maintain this test program across a variety of test platforms.

Fortunately, you can avoid this cumbersome and costly approach by handling the comparison between analog values and acceptable limits using on-chip limit registers. The first

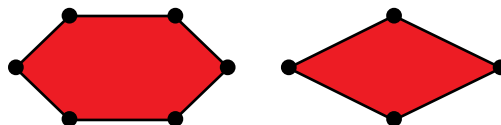


Figure 4 You can automate eye-mask tests by specifying voltage and phase values for various points on a hexagonal or diamond mask. Compare registers that connect to your SOC's on-chip analog-test bus can automatically determine whether your specified eye values match the actual values of the on-chip signals. In the six-point mask (left), the six points yield a voltage of 100 mV and a phase of 0.2 unit intervals, a voltage of 100 mV and a voltage of -0.2 unit intervals, a voltage of -100 mV and a phase of 0.2 unit intervals, a voltage of -100 mV and a phase of -0.2 unit intervals, a phase of 0.4 unit intervals, and a phase of -0.4 unit intervals. A four-point mask (right) yields a voltage of 100 mV, a voltage of -100 mV, a phase of 0.4 unit intervals, and a phase of -0.4 unit intervals.

step is to simply write into the chip the high and low analog limits and the instructions to measure the desired value. Each test sets an on-chip pass/fail bit that you can then scan for a simple pass/fail comparison. You need not write a test program; you need only software to create the input and compare vectors, just as in conventional digital scan. The result of placing the limit registers and ADC on-chip is true analog testing on any simple digital tester on any test platform.

To make on-chip analog-test capabilities as easy to use as digital-scan methodologies, software tools must convert typical analog tests to digital-test patterns. The software must be able

to generate pass/fail tests that would otherwise require a large amount of configuration and circuit knowledge.

With the increasing availability of PHY interfaces as IP, the IP industry must implement digital testing of emerging serial interfaces in a straightforward way. This implementation will allow IP users to quickly assemble complete analog-test suites without an in-depth knowledge of the IP or of a serial-interface standard.

As an example of such a test implementation, consider the typical eye-mask test. The relevant interface standard specifies eye masks that provide a starting point, but designers usually use a larger mask to account for channel distortion and to ensure interoperability (**Figure 3**). Using a diamond or hexagonal mask, a designer specifies pass/fail values for voltage and phase for each point on the mask (**Figure 4**). The software then generates the appropriate vector to place the device in the proper configuration and applies the specified mask. The SOC then returns a pass/fail result. This approach to testing requires no device knowledge.

FULL-TIME VISIBILITY

In addition to providing a low-cost test method, on-chip test also allows for in-the-field debugging and testing. Circuitry should display eye diagrams at the receiver and measure various other critical parameters. This capability provides an easy method to help evaluate field issues. With transmitter pre-emphasis and receiver equalization becoming ever more popular,

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the ability to measure the effects of various settings on a link at any time is valuable.

The conventional approach of production testing using simple external loop-back is fast but inaccurate. On the other hand, expensive, sophisticated mixed-signal testers burden users with additional overhead costs and the need to write and debug complex test programs. With the help of on-chip analog-test circuitry, you can test high-speed serial interfaces at speed on a low-cost digital tester in little time. As a result, you can generate verified pure-digital test patterns for compliance tests and other requirements, including eye mask, asynchronous-voltage margining, and transmitter-level testing. Further, you can use this same circuitry to aid in debugging and characterizing such interfaces. **EDN**

AUTHOR'S BIOGRAPHY



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