BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

IP selection and power supplies

With the "greening" of electronics and IC systems, power-supply strategies are critical portions of the IP (intellectual-property)-selection process. There are two major competing power-analysis standards in the EDA world: the Accellera (www.accellera.org)-coordinated UPF (Unified Power Format) and the Cadence (www.cadence.com)/Si2 (www.si2.org)-coordinated CPF (Common Power Format). Application organizations, such as the Consumer Electronics Association, also drive power-measurement and -analysis standards. In response to the multiple formats, IP providers have not fully adopted any one side to avoid the risk of limiting their potential client bases. This failure to fully embrace just one of the standards, however, has caused confusion and uncertainty in IP users about power-strategy compatibility.

This uncertainty is a problem for several reasons. First, design groups need power-supply standards because they are trying to enhance the RTL (register-transfer-level) netlists by including power supplies in their connectivity. As a result, the design groups need to understand the source and management of the power.

More important, as the designs are going green, multimode power is key. Once again, there is variety: IP developers use several power-management techniques in different applications and for different circuits. For dynamic-power management, designers might employ simple logic optimization, clock gating, multithreshold voltage, or DVFS (dynamic-voltage and frequency scaling). Power gating, multithreshold design, and multithreshold CMOS are methods designers might employ for leakage-power management. It is difficult and consumes a great deal of conversion logic to have a large function comprising multiple IP blocks using multiple power-management techniques.

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Because there are multiple power solutions, and because these approaches have backing from different EDA vendors, you have to make sure that your IP is compatible with the EDA tools you are using. Both the UPF- and the CPF-specification formats have recommended methods, tools, and techniques for dealing with logic, clocks, and memories, as well as with other hard-IP blocks. However, the formats do not contain the same information and do not guarantee conformance or interoperability of blocks from different IP suppliers at different stages of the design process on different tools. You can obtain information from www.accellera.org/activities/upf and www.si2.org/?page=811.

From a functional point of view, the most important aspect of the power management for a design is the long-standing issue of process-isolation techniques for the applications of power. Power-reduction requirements notwithstanding, it is still important that fast-switching, high-noise power is not near or connected to high-sensitivity circuits. For that reason, designs still need multiple functional power rails for core power, memory power, I/O power, analog power, display power, and the like.

One of the last issues for IP selection—and one that designers often miss—is the type of package that will house the end product. Traditional designs employ edge-oriented I/Os, which use standard interconnect techniques to get from the circuit to the power pads. A large number of high-pin-count designs use core I/O, which is a generic term for pads that are in the middle of the chip directly over active circuitry. Designs that use core I/O can have just power supplies, just signals, or both power supplies and signals on these pads. The IP blocks must accommodate the effects of the mechanical stress that both the pads and the pads' electrical-performance issues cause. A recently emerged option that is increasingly popular for mobile and small-form-factor applications is the use of TSVs (through-silicon vias) in and around IP blocks. TSVs for stacked and 3-D die interconnect have significant die-to-die modeling and verification issues. You must develop third-party IP for applications that will employ TSVs in close cooperation with the IP provider and system-design group. EDN

Contact me at pallabc@siliconmap.net.

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