

# HANDCRAFTED ANALOG GETS AUTOMATED ASSIST

EDA TOOLS ADDRESS SIMULATION, VERIFICATION, AND LAYOUT FOR MIXED-SIGNAL DESIGNS.

**A**nalog simulators and design-capture tools have a venerable history in the EDA market, having long added some Spice to their digital-simulation counterparts. When it comes to converting simulations to sine waves and silicon, however, analog-EDA tools fall short of what has been possible in the digital domain. That scenario is beginning to change. Tools are emerging from traditional digital-EDA providers that support the fabrication of analog functions in nanometer-geometry digital processes. In addition, foundry-specific tool kits are easing the implementation of analog, RF, and high-voltage functions in analog processes.

Designers cannot expect smooth sailing, though; full automation of analog- and mixed-signal design remains elusive. Even analog-Spice engines may run out of steam as chips become more complex, requiring excessive times for full-chip simulation, even with fast-Spice implementations. Nevertheless, vendors are working on multiple fronts to bring automaton to the traditionally handcrafted analog-design task.

One way to deal with analog design is to reformulate analog problems as computational ones. Justin R Rattner, vice president and chief technology officer at Intel, suggested that approach, digitally assisted ana-

log, during this year's DAC (Design Automation Conference) keynote address (**Reference 1**). Not all problems are amenable to digital computational solutions, however. You can't readily "calculate" a 120V signal level, no matter how many 45-nm digital transistors you throw at the problem. And, apart from voltage and current levels, the need for analog functions isn't going away. As Texas Instruments Senior Vice President Gregg Lowe points out, the transition to digital—for instance, music's transition from vinyl to MP3—results in an increase in analog content (**Reference 2**).

The need for more analog content

mandates better analog-design tools. Mar Hershenson, vice president of product development at Magma Design Automation's custom-design-business unit, describes analog design as it has occurred over the last 20 years as the work of artists, with engineers manually designing op amps and other analog functions. As if analog design weren't difficult enough, she adds, integrating the analog and the digital portions of a mixed-signal design can take weeks. Further, for every process node, analog-system engineers must manually re-create designs.

And even ICs that are functionally digital—that is, producing no signals other than zeros or ones—are exhibiting behavior that requires analog-design and -test techniques. That situation is particularly true of the high-speed serial interfaces that let chips communicate with the outside world.

## IP AND ANALOG BEHAVIOR

The term *analog* conjures up visions of op amps and data converters, but, explains Navraj Nandra, director of marketing for mixed-signal IP (intellectual property) at Synopsys, "The speeds of today's chips' serial-digital-I/O lines ensure that analog effects come into play" even in





ostensibly all-digital parts. Complicating matters, he says, is that pure-analog companies have the luxury of implementing functions in processes optimized for analog circuitry. In contrast, companies making digital chips want to implement their high-speed I/O in standard deep-submicron digital processes—with all the attendant process-variation and signal-integrity issues.

Synopsys addresses serial-I/O-design problems with its DesignWare IP to implement functions, such as USB 2.0, DDR2/3 memory, SATA (serial-advanced-technology-attachment), and PCIe (peripheral-component-interconnect-express) 2.0 interfaces. The DesignWare PCIe 2.0 product, for example, includes the PHY (physical-layer interface), operating at 5 Gbps, as well as a digital controller and verification IP. Nandra notes that Synopsys has successfully produced a USB 2.0 PHY in 65-nm processes at fabs Chartered Semiconductor, Samsung, and IBM—all with a single GDSII (graphic-design-system II) file with no modifications.

IP isn't useful if it isn't testable in the lab or on the production floor. For lab tests, Synopsys obtains split-lot samples from foundries and evaluates them using demo boards, performing eye-diagram-mask tests using bench-top oscilloscopes (**Figure 1**). For production test, Synopsys builds diagnostic IP into its PHYs—essentially on-chip sampling oscilloscopes accessible through a JTAG port, enabling a conventional digital tester to perform real-time eye-diagram-mask testing. Nandra elaborates on the on-chip test technology in **Reference 3**.

### MIXED-SIGNAL FLOWS

The ultimate goal of mainstream-EDA companies is to bring what they might perceive as the pushbutton ease of operation of digital-design flows to analog- and mixed-signal design. Mixed-signal design, says Steven Lewis, product-marketing director at Cadence Design Systems, has traditionally involved forcing the analog domain within the digital domain or vice versa. Citing the comments of Intel's Rattner regard-

### AT A GLANCE

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ing digitally assisted analog, Lewis says that forcing one domain into another is becoming untenable. "At 65 and 45 and 32 and 22 nm, you have this blurring of lines," he says. "It's not so obvious where the analog and digital pieces begin and end."

An isolated analog/digital approach is no longer sufficient and must give way to approaches that permit top-down design and that let customers mix methodologies, according to Sandy Mehndiratta, group director for custom ICs at Cadence. Lewis adds that an effective design strategy must also support multiple

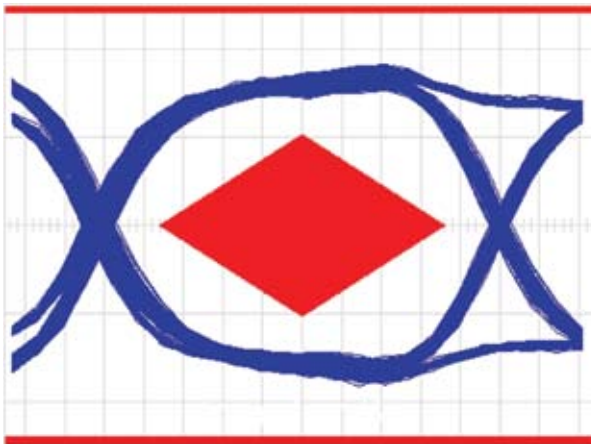
geographically dispersed design teams having diverse skills.

The Cadence approach, says Lewis, is "to build an umbrella solution" that allows engineers to work in whichever domain makes the most sense for them. To that end, Cadence works to break down the boundaries between analog and digital verification as well as analog and digital implementation (**Figure 2**).

To allow each domain to understand the other without translation, the implementation stage, for instance, brings Cadence Virtuoso and Cadence Encounter together under Si2's OpenAccess, which Lewis describes as necessary but insufficient for an effective mixed-signal flow. Cadence engineers have brought Virtuoso and Encounter together, ensuring the maintenance of digital connectivity during analog editing and the locking of analog portions during digital-floorplanning adjustment. Within the combination, Encounter supports PCells (parameterized cells), multipart paths, and guard rings. Lewis says that a customer has reported a 25% reduction in overall mixed-signal-design-cycle time.

Magma based its approach on technology it obtained with the February acquisition of Sabio Labs. Magma's Hershenson, who was formerly chief executive officer of Sabio, says that the technology accelerates mixed-signal- and analog-design migration through Magma's Titan Chip Finishing and Titan Analog Migration platforms. Titan employs a unified-database architecture and supports fast shape-based routing and full-layout editing; it includes a complete encapsulation of Magma's Talus digital-design platform and Quartz DRC (design-rules-checking) and Quartz LVS (layout-versus-schematic) verification tools. Titan can also instantiate PCells.

Magma integrates the Titan Analog Migration platform with the company's FineSim, which in turn supports multi-CPU Spice simulation. Titan Analog Migration allows engineers to migrate their analog designs from one process node to another in a matter of hours, says Hershenson. Indicative of



**Figure 1** An eye-diagram-mask test illustrates the performance of Synopsys PHY IP for PCIe 2.0. You can directly observe the diagram on an oscilloscope from a demo board; for production test, an internal sampling-scope function makes the eye diagram available to a standard digital ATE (automatic-test-equipment) system through a JTAG port.

Titan Chip Finishing's speed, she said it can open a 42-Gbyte file in 4 minutes and can redraw a full chip in 8 seconds.

Mentor Graphics' approach is to bring together design-implementation and -verification tools into an analog/mixed-signal-design flow that a data-management system governs (Figure 3), according to Min-Fang Ho, general manager of Mentor's custom-IC division. The Design Manager data-management tool allows users to collaborate among multiple sites or handle revision control. Other components include Design Architect IC for schematic capture, IC Station and ICassemble layout and assembly tools, Eldo and ADiT simulators, and Calibre physical-verification tools.

Henry Chang, Mentor's director of marketing for analog- and mixed-signal tools, elaborates on the simulation portion of the flow. Eldo is a Spice-based simulator, Eldo RF adds RF extensions, and ADiT is a fast Spice simulator that trades some accuracy for speed. Mentor's ADVance tool, he says, brings together those simulators and combines them with Mentor's ModelSim digital simulator to verify complete mixed-signal designs.

IDMs (integrated-device manufacturers) and foundries also offer mixed-signal-EDA tools. Austriamicrosystems, for example, offers the HIT-KIT (high-performance-interface-tool kit)—a utility comprising software programs and libraries that support behavioral simulation, digital synthesis, schematic capture, mixed-signal simulation, layout, design verification, and back-annotation within Cadence, Mentor, and Synopsys design environments. According to Thomas Riener, general manager of austriamicrosystems' full-service-foundry-business unit, the kits provide a consistent user interface for the company's internal designers and foundry customers. Thomas Mörth, manager of design support at the foundry-business unit, notes that the kits add custom features, such as the ability to verify that, with

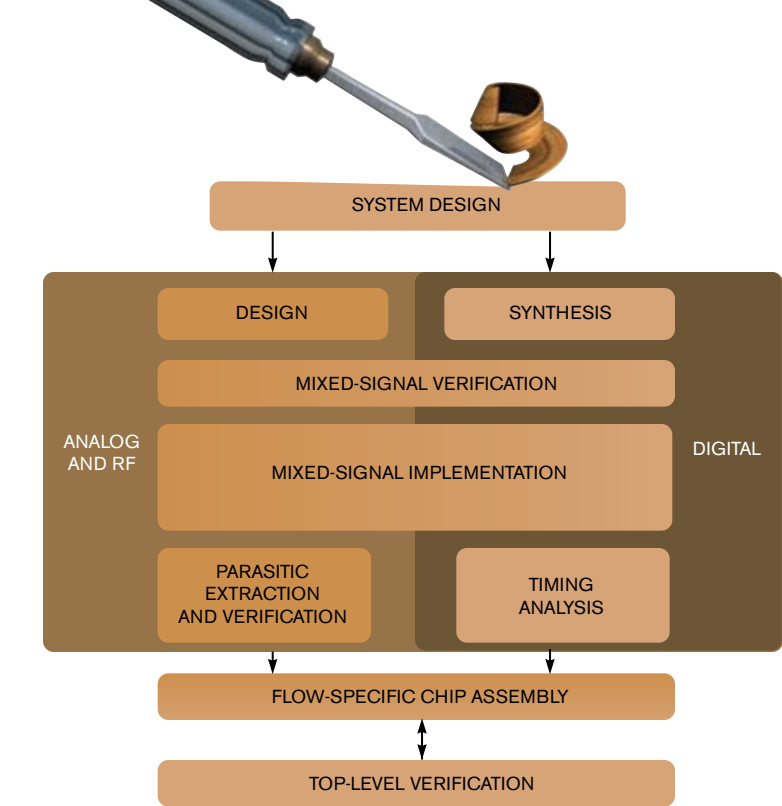


Figure 2 Breaking down the boundaries between analog and digital verification and implementation is the goal of Cadence's mixed-signal-design flow. The implementation stage, for instance, brings together Virtuoso and Encounter under OpenAccess, allowing each domain to understand the other without translation.

transistors operating at 3.3, 20, 50, and 120V on a single die, each transistor remains within its safe operating range.

### LOOKING TO THE FUTURE

As for what designers would like to see from EDA companies, topping the list are multithreaded versions of Spice that can take full advantage of multicore processors. Austriamicrosystems' Mörth notes that, although some Spice implementations use multiple cores, they generally rely on a single core to solve the set of matrix equations that describe the simulated circuit. "You can buy more and more hardware, but it gets to a point where that no longer helps," says Riener. "If you want to do a top-level simulation that takes three weeks, it will continue to take three weeks no matter how many CPUs you add to your server farm."

Steven Daniel, worldwide R&D manager of the analog, mixed-signal, and power division at Freescale Semiconductor, and Erwan Hemon, the worldwide automotive-IC-creation manager at the same division, also would like to see faster simulators. "Top-level simulation of a full chip with analog and digital

components is a long and difficult process that can take a month at minimum and is not user-friendly," says Hemon. The process needs acceleration through parallel-processing support.

Freescale engineers employ many proprietary, in-house design-automation tools that provide leading-edge performance not available from commercial tools, but Hemon notes that a commercial tool could be a viable alternative once an internal tool has lost its ability to provide differentiation. Daniel and

### FOR MORE INFORMATION

**austriamicrosystems**  
www.austriamicrosystems.com

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**Design Automation Conference**  
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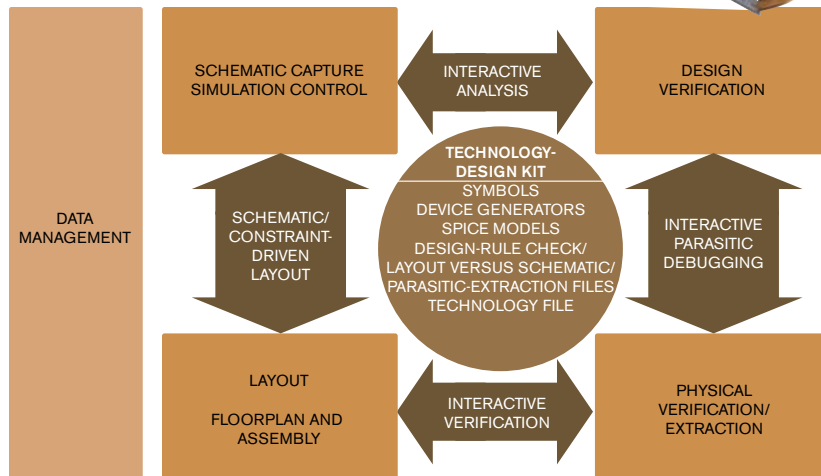
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**Figure 3** Allowing users to collaborate among multiple sites, Mentor Graphics' Design Manager data-management tool orchestrates an interactive analog/mixed-signal design flow. Within the flow, Design Architect IC handles schematic capture and simulation control; IC Station and ICAssemble perform layout, floorplanning, and assembly; Eldo, ADiT, and ICAnalyst handle design verification; and Calibre DRC/LVS and Calibre xRC handle physical verification and extraction.

Hemon list several features they would want to see in commercial tools: support for high-voltage transistors, not just low-voltage CMOS transistors; the ability to model ESD (electrostatic-discharge) effects; and the ability to predict defect rates and aging effects. To capture defects in the analog portion of mixed-signal silicon, Hemon says Freescale engineers would like to develop a test methodology similar to the digital domain's IDDQ (integrated-circuit-quiescent-current) test. Finally, they would like to see test-program-generation support.

EDA vendors aren't specific about what's just over the horizon, but Cadence's Lewis says his company is looking at bringing assertion-based approaches—common in the digital world—to facilitate verification and test of mixed-signal designs.

Mentor's Ho says that efforts are under way to improve the communication of design intent from the schematic-capture and simulation area to the implementation area. Such an approach would invoke principles and guidelines that would facilitate automation of some tasks but still provide flexibility. Chang says that, to support mixed-signal design and implementation at 45-nm process nodes, foundries and EDA companies will need to work closely together to de-

velop complex device models that designers can efficiently simulate. Finally, Ho notes, printability issues are affecting designs at 40 nm, and manufacturers might better address those issues at the design stage rather than through RET (reticle-enhancement-technology) and OPC (optical-process-correction) techniques. **EDN**

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You can reach  
Editor-in-Chief  
**Rick Nelson**  
at 1-781-734-8418  
and [rnelson@reedbusiness.com](mailto:rnelson@reedbusiness.com).

