EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

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Linear wind-power meter compensates for temperature

W Stephen Woodward, Chapel Hill, NC

The rise of interest in renewable energy created by soaring fossil-fuel costs and global-warming fears has created a matching interest in associated support and demonstration instrumentation. This Design Idea hops on that bandwagon with the ability to directly and conveniently measure an important renewable-energy source: wind power. Handy for quick and easy preliminary evaluation of potential wind-turbine sites, it includes a wind-speed transducer, comprising an optically sensed vane anemometer, and a temperature sensor, comprising a diode-connected transistor. These components interface with a hybrid digital/analog-computation circuit. In combination, they provide a real-time, linear, temperature-compensated readout of wind-power density.

The power-generation potential of wind is ½×air density (kg/m³)×air speed (m/sec)³. To compute it, there-

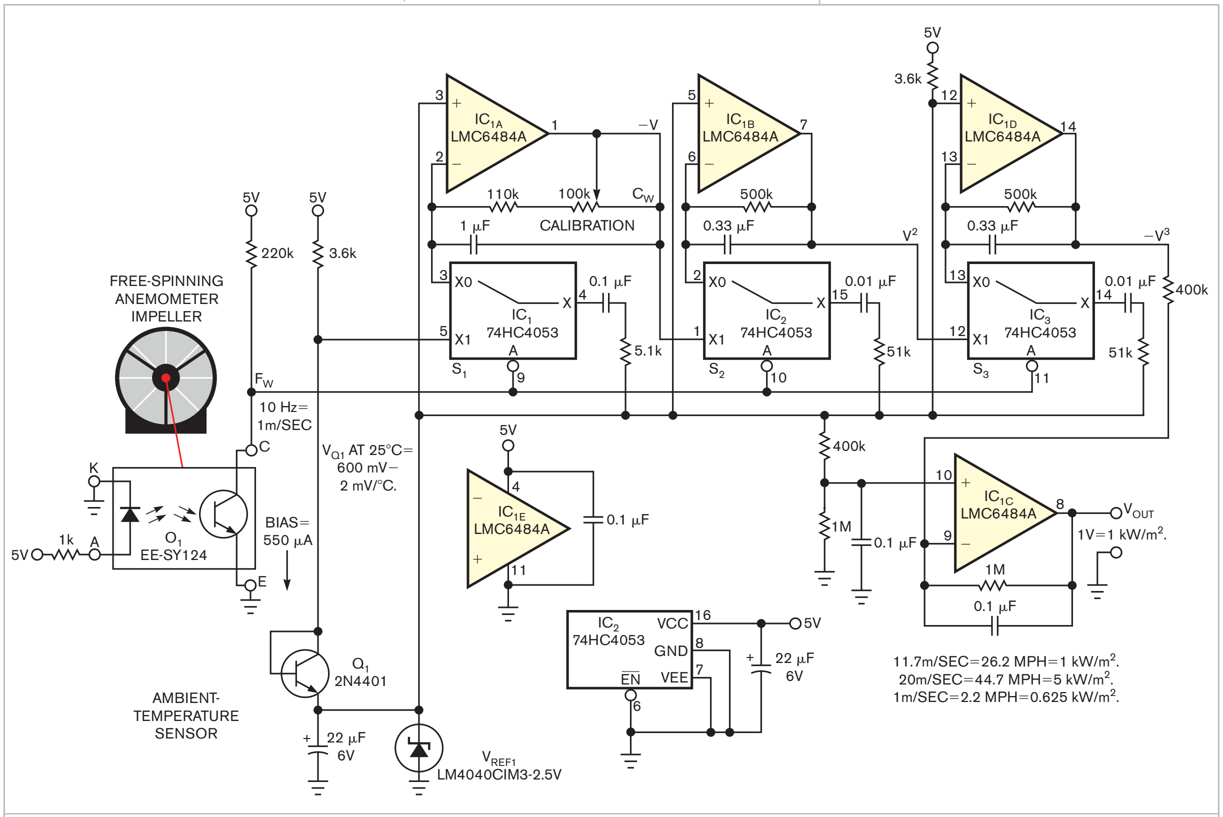


Figure 1 This meter circuit uses a free-spinning anemometer and a diode-connected transistor temperature sensor to measure the available wind power for "green" power generation.

fore, requires estimating air density, which is inversely proportional to absolute temperature; measuring air speed; and calculating a cube.

Here's how the wind-power meter does it. Diode-connected Q_1 has a bias of 550 μA for a 25°C (298K) base-to-emitter voltage of approximately 600 mV and a temperature coefficient of −2 mV/°C. Thus, Q_1 is a voltage reference that tracks the approximate ideal-gas-law temperature dependence of air density: −0.3%/°C. Meanwhile, optical sensor O_1 works with a free-spinning anemometer impeller to produce wind-speed-proportional frequency: F_W=10 Hz/m/sec. Conversion of V_{Q1} and F_W into a 1-mV=1W/m² output signal is then the function of the third-order X×Y×Z-multiplying behavior of three cascaded CMOS-switch FVC (frequency-to-voltage-converter) charge pumps: S_1, S_2, and S_3.

FVC S_1/IC_{1A} generates a negative voltage of $-0.17\times V_{Q1}\times F_W$; FVC S_2/IC_{1B} generates $V_2=-V\times F_W=0.17\times V_{Q1}\times F_W{}^2$; and FVC S_3/IC_{1D} generates $-V_3=-0.17\times V_{Q1}\times F_W{}^3$. Finally, differential inverter IC_{1C} shifts and scales $-V_3$ to output $V_{OUT}=0.42\times V_{Q1}\times F_W{}^3=1V/kW/m^2$.

You can conveniently calibrate the wind-power meter in an automobile being driven on a windless day at a constant speed of 18.6m/sec=41.5 mph=66.8 kph. With the anemometer exposed to the external slipstream, adjust the calibration trimming potentiometer for an output voltage of 4V or, for better accuracy, to the voltage that the following formula that accommodates true air density yields: V_{OUT}=1.14V×air-pressure millibar/(273+ambient temperature Celsius).EDN

Oscillator uses dual-output current-controlled conveyors

Abhirup Lahiri, Netaji Subhas Institute of Technology, New Delhi, India

In the last decade, engineers have done much work in designing and implementing current-mode circuits using second-generation current conveyors, which have higher signal bandwidth, greater linearity, larger dynamic range, simpler circuitry, and lower power consumption than their predecessors. Recently, a second-generation dual-output, current-controlled conveyor has emerged. The device is an active building block (**Figure 1**), and the following equations characterize it: $I_Y=0$, $V_X=V_Y+I_XR_X$, and $I_{Z+}=I_X$; $I_{Z-}=-I_X$. The parasitic resistance at terminal X is $R_X=(V_T/2I_B)$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades.

Figure 2 shows current-controlled oscillators with few components, employing only two dual-output current-controlled conveyors and two grounded capacitors. The devices use no external resistors, and the parasitic resistance at terminal X realizes resistance. The proposed design for the circuit provides electronic controllability of frequency of oscillation.

The characteristic equation for both of the circuits in **Figure 2** is $s^2C_1C_2R_{X1}R_{X2}+sC_2R_{X1}-sC_1RX_1+1=0$. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360°—the required condition for oscillation is $C_1=C_2$, and the frequency of oscillation is $f=1/(2\pi\sqrt{C_1C_2R_{X1}R_{X2}})$.

Assuming that $C_1=C_2=C$ and taking $R_{X1}=R_{X2}=V_T/2I_B$ yield a frequency of oscillation: $f=(I_B/\pi CV_T)$. Clearly, the dc-bias current, I_B, can vary the frequency of the current conveyors, and the frequency is, therefore, electronically controllable.EDN

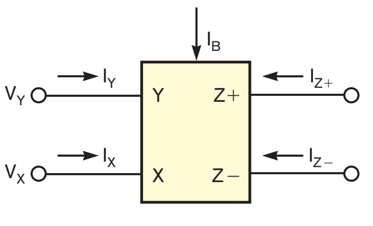


Figure 1 This dual-output current-controlled conveyor illustrates the quantities the equations use.

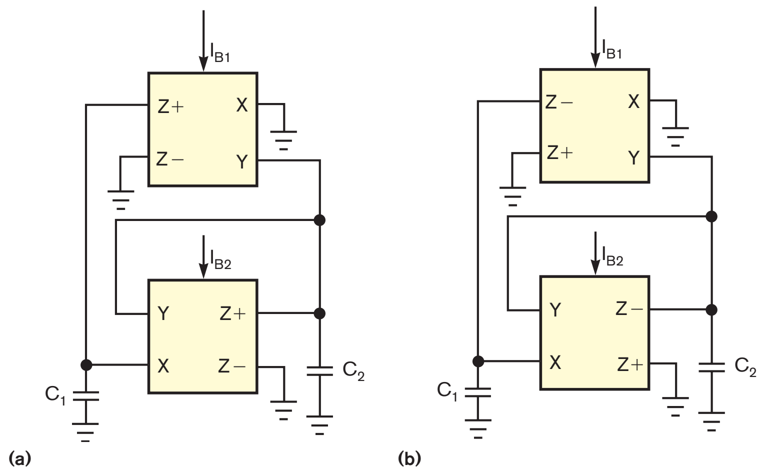


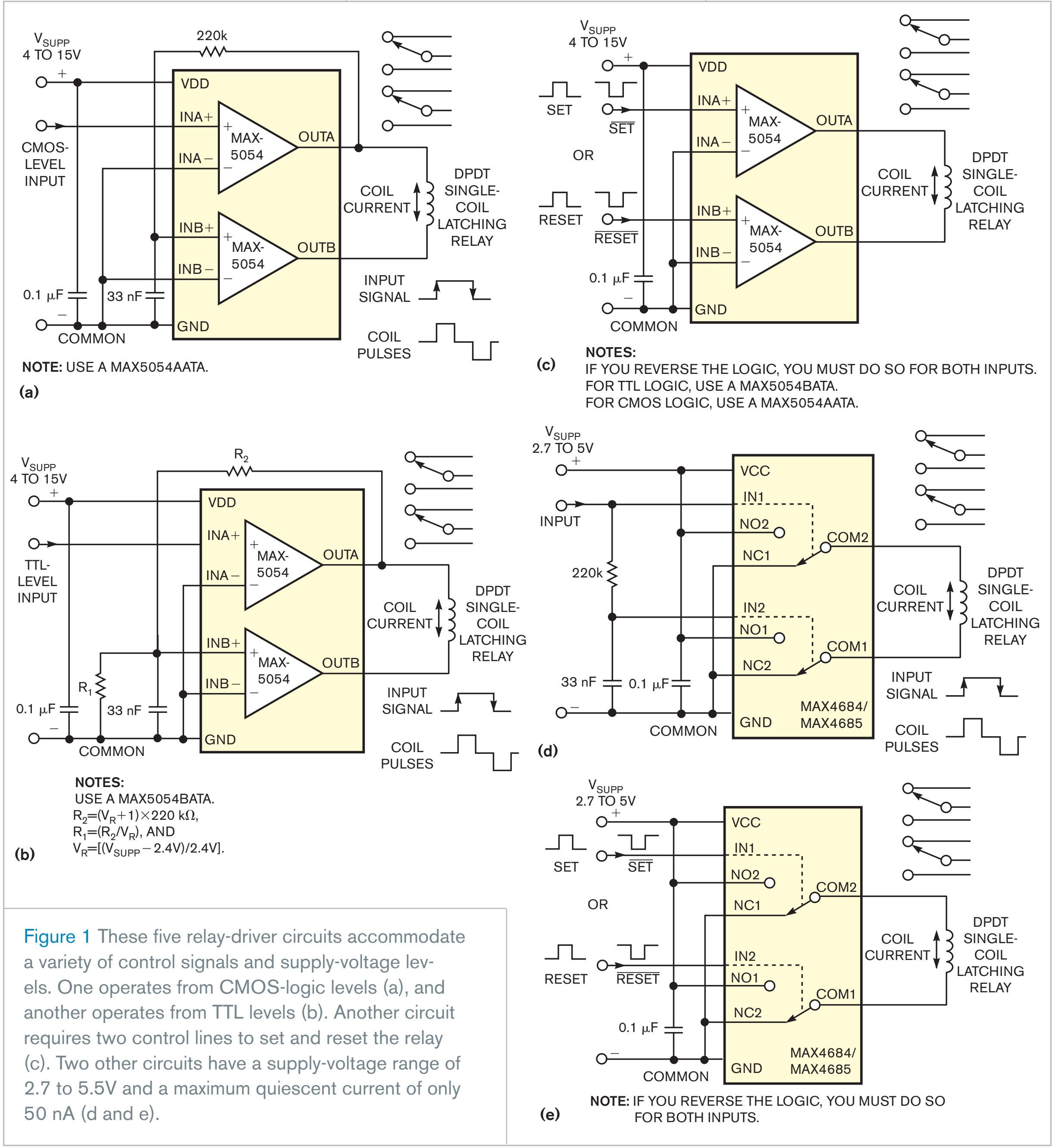
Figure 2 Varying the bias current, I_B, of the dual-output current-controlled conveyor (a) controls its frequency of oscillation versus another device (b).

Circuits drive single-coil latching relays

Alfredo H Saab and Tina Alikahi,
Maxim Integrated Products, Sunnyvale, CA

A single-coil latching relay is a relay with memory, usually with a magnetic structure that provides two stable positions for the armature that holds the movable contacts. A permanent magnet provides the force holding the armature in these stable positions. An application of electrical current to the relay coil moves the armature from one position to the other, which in turn changes the contact positions.

Applying to the coil a current pulse in one direction, of longer duration than the specified minimum for that relay type, sets the relay to the first of two stable positions, and it remains in that position after the current ceases to circulate. Current in the opposite direction resets the relay to the other position, which is also stable with no current. The relay then indefinitely remains in that position until a new current pulse toggles it to the other position.



NOTE: USE A MAX5054AATA.

NOTES:
USE A MAX5054BATA.
$R_2=(V_R+1)\times220\ k\Omega$,
$R_1=(R_2/V_R)$, AND
$V_R=[(V_{SUPP}-2.4V)/2.4V]$.

NOTES:
IF YOU REVERSE THE LOGIC, YOU MUST DO SO FOR BOTH INPUTS.
FOR TTL LOGIC, USE A MAX5054BATA.
FOR CMOS LOGIC, USE A MAX5054AATA.

NOTE: IF YOU REVERSE THE LOGIC, YOU MUST DO SO FOR BOTH INPUTS.

Figure 1 These five relay-driver circuits accommodate a variety of control signals and supply-voltage levels. One operates from CMOS-logic levels (a), and another operates from TTL levels (b). Another circuit requires two control lines to set and reset the relay (c). Two other circuits have a supply-voltage range of 2.7 to 5.5V and a maximum quiescent current of only 50 nA (d and e).

The electronic circuitry to drive one of these relays from logic signals can be a half-bridge if dual supply voltages are available or a full bridge—that is, an H-type power driver—if only a single supply voltage is available. The need to generate reversible-current pulses through the two-terminal coil imposes the use of these bridge topologies. Because the relay itself does not consume power under static conditions, the driving circuitry should also consume minimal power under the same conditions.

Figure 1 illustrates a variety of driving circuits, depending on the input-signal-logic levels, their coding, and the magnitude of the available supply voltages. The circuits in **figures 1a** through **c** drive relays for voltages of 4 to 15V. The circuit in **Figure 1c** requires two separate control lines: The set line sets the relay, and the reset line resets it. You can code the set and reset signals as positive (active high) or negative (active low). You must use the same logic convention for both inputs in this circuit.

The widths of the set and reset signals must be longer than the minimum time required for the relay to operate—typically, 3 to 5 msec. For proper operation, you should apply only one signal at a time; while applying one, the other should remain at the nonactive-logic value. Using positive logic, for example, the signal must go high for 3 to 5 msec, and the other input must remain low until the first signal pulse ends. The choice of IC determines the logic level: TTL (transistor-to-transistor logic) or power-supply-level CMOS (**Figure 1c**).

The circuits in **figures 1a** and **1b** operate from a single on/off-signal line, generating a coil-current pulse with each transition of the input signal. The polarity of the coil-current pulse depends on the polarity of the input-signal transition that generates it (**figures 1a**, **b**, and **d**). The circuit in **Figure 1a** operates from CMOS-logic levels, and the one in **Figure 1b** operates from TTL levels. After each transition, the signal must remain stable for longer than the relay's minimum operating time. The circuits in **figures 1a** and **c** typically draw quiescent currents of 40 μA, and the one in **Figure 1b** typically draws approximately 50 μA. The circuits in figures **1d** and **1e** are similar to those in **figures 1a**, **1b**, and **1c**, but their supply-voltage range is 2.7 to 5.5V, and their maximum quiescent current is only 50 nA.

Because the single-coil latching relay has a memory of its own, you must initialize its position after power-up to a known state, either by exercising the input logic or by analyzing and responding to a signal from the contacts' circuitry. Any of these circuits can deliver as much as several hundred milliamps in either polarity while pulse-driving a relay coil. You can find technical information and data sheets for the ICs in these circuits at www.maxim-ic.com.EDN