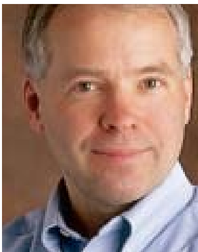

BY RICK NELSON, EDITOR-IN-CHIEF

From lithography to test

This year, I commented on the importance of taking test into account during the design phase (**Reference 1**). Examples I cited included Asset InterTech's focus on providing open tools for embedded instrumentation in design-validation, test, and debugging applications. The company reiterated that focus last month at the ITC (International Test Conference) in Santa Clara, CA, when it announced that it has joined the Synopsys in-Sync program to gain access to Synopsys' Galaxy test tools. For its part, Cadence Design Systems announced at ITC that Moai Electronics has made joint use of the Cadence Encounter RTL-(register-transfer-level) Compiler design tool and Encounter Test design-for-test tool to tape out a flash-memory controller, reducing RTL-to-ATPG (automatic-test-pattern-generation) turnaround time from weeks to days.

Test—one of the last steps to take place before product shipment—isn't the only aspect of semiconductor production that designers should address for optimum results, however. Designers must also take into account manufacturing issues that appear as early as the lithography stage. That fact became clear at a research-review meeting held in October at ASML in Veldhoven, the Netherlands. At the meeting, presenters discussed the importance of computational lithography in, for example, producing 22-nm features using 193-nm light waves—that is, "creating thin lines with a broad brush," said Neal Callan, ASML's vice president for marketing and product development.

The need for manufacturing-aware design tools is not new, and EDA companies have been addressing the issue, as I noted in a blog post more than two years ago (**Reference 2**). The need for the OPC (optical-proximity-correction) DFM (design-for-manufacture) technique kicked in when processes approached 130 nm, said Callan at the meeting. And it's becoming increasingly important as lithography companies turn to double-patterning as an interim approach that will serve until EUV (extreme-ultraviolet) lithography becomes available, which is expected to be in 2010, according to ASML fellow Jo Finders.

Finders described the double-patterning flow, which requires dividing a layout into two patterns for the production of two masks, with patterns recombining through double exposure of the target die. Successful application of the technique, he said, depends on an overlay-friendly layout that in turn depends on effective DFM tools.

ASML is addressing double-patterning with its recently introduced Twinscan NXT platform, which the company says will enable manufacturers' need to shrink their smallest chip features by as much as 42%. ASML addresses the DFM aspect through its Brion subsidiary, which it acquired in 2007. Suggesting how complex the technology is, Callan noted the need to optimize not only the mask but also the light source to produce the best images. The forte of Brion and competing DFM organizations is mask optimization through OPC and other techniques. To address double-patterning in particular, Brion's approaches, Callan said, provide gate-aware splitting of images and ensure density balance between two corresponding patterns.

Callan noted that computational lithography depends on accurate modeling and, not surprisingly, that Brion's intimate knowledge of ASML scanners enables better image prediction. However, ASML doesn't intend to keep all its scanner knowledge to itself. Through Brion, Callan said, ASML will proliferate ASML scanner models throughout the DFM value chain through the VSP (Virtual Scanner Pack), which will be available to EDA companies, including Cadence, Magma Design Automation, Mentor Graphics, and Synopsys. Customers who use design or computational-lithography tools from any company can access ASML scanner models through the VSP, which should benefit chip-design software companies as well as chip manufacturers. EDN

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