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## Mentor's new DRC tool targets 32-nm node

**M**entor Graphics is enhancing its market-leading Calibre physical-verification environment for subwavelength-semiconductor processes with Calibre EQDRC (equation-based design-rule checking). The equations can be multivariable statements, which Calibre calculates dynamically using other measurement criteria, as part of the DRC. Traditional DRC programs have short-range, fixed-condition, single-measurement-value rules (Table 1, available in the Web version of this column at [www.edn.com/081205pc](http://www.edn.com/081205pc)). Designers typically use these rules for 0.35- $\mu\text{m}$  or larger-geometry processes.

Combinations of rule- and model-based rules are typical for 0.25- $\mu\text{m}$  to 65-nm process technologies. Conditional, critical-area-analysis, and complex-2-D rules, as well as staggered “if-then-else” loops, validate geometry in these technologies. Using all these types of rules has led to an explosion in the size of the runtime code to support complex, multilayer, and multi-property design rules. In larger processes, this type of rule was the exception, but, in 45-nm and smaller processes, it is the norm.

Mentor created the Calibre EQDRC environment to optimally support 32-nm processes and validated the rule sets with a major commercial-32-nm-CMOS-process foundry. The company is not unique, however. Synopsys also implemented an addition, targeting the 45-nm node, to its runtime syntax for the Hercules DRC/LVS (layout-versus-schematic) tool. No one knows when or whether customers will adopt any geometry smaller than 45 nm, however.

Thanks to its support for multivariable-mathematical expressions, the new syntax supports complex-rule implementation with significantly less code. The syntax also allows for systematic support of implicit and suggested design rules. As a result, designers can test the guidelines for multivoltage designs, latch-up resistance in multipower-state designs, and core-I/O-stacking rules.

Figure 1 shows a typical application of a simple mathematical solution and

runtime coding for a spacing rule that involves CMP (chemical-mechanical-polishing) dishing and metal spacing. This approach replaces more than 50 lines of SVRF (standard-verification-rule-format) coding and has a faster runtime in a smaller memory footprint than standard coding. Another example from Mentor replaces more than 3000 lines of customer-derived runtime code with fewer than 30 lines of enhanced coding to support alignment of vias and via-count rules. Most of the applications address application DFM (design-for-manufacturing) and lithography prescreening rules.

Because the rules do not directly relate to the design objects, multiple conditions may be at work for the design checks, meaning that error reporting also changes. The tool not only flags the offending object—that is, the edge, vertex, or polygon—as an error but also highlights repair options. For instance, the tool may base a position rule on an edge location, an overlap, or a corner rule and present all three repair options so that the user can choose the most appropriate one for the design application. This feature should significantly reduce the debugging time and learning curve for new processes for the physical-design staff. **EDN**

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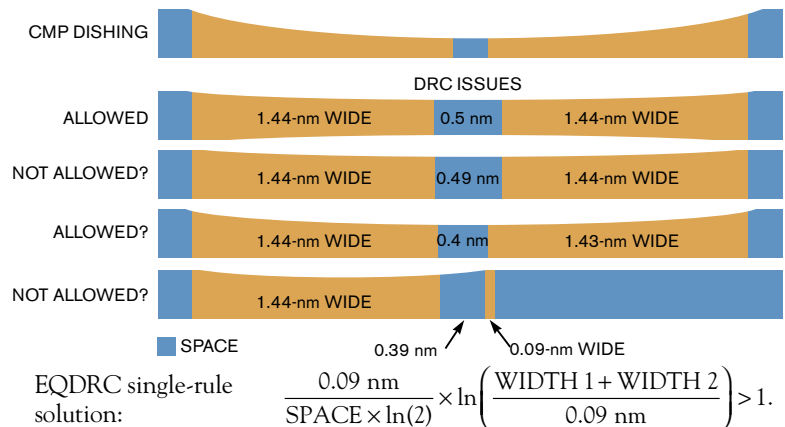


Figure 1 With EQDRC, you can replace more than 50 lines of standard coding with one rule.