



BY BONNIE BAKER



# What's in your SAR-ADC application?

“Finding an amplifier that doesn't tarnish an ADC's performance is hard enough. But now you also have to deal with single-supply voltages and the quirky switched-capacitor input structure” (Reference 1). Engineers have been struggling with the task of driving the SAR (successive-approximation-register)-ADC, charge-redistribution, or C-DAC (capacitive-data-acquisition-converter) input architectures for more than a decade.

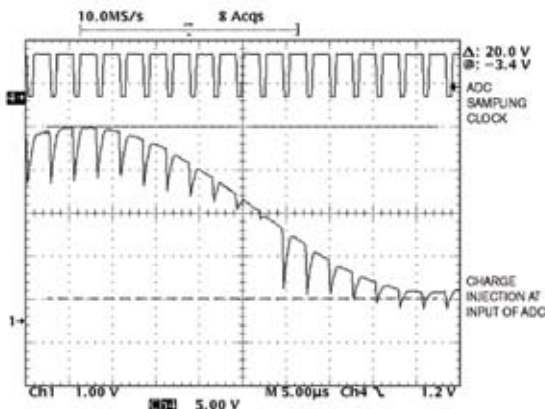


Figure 1 By placing a 10-kΩ resistor between a buffer op amp and a SAR-ADC input, you can see the ADC charge-injection action.

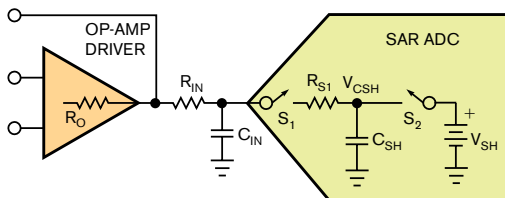


Figure 2 Choose an amplifier with an input range that is appropriate for the input-signal requirements, then connect the amplifier through an RC system to the ADC.

Driving a SAR ADC with an amplifier seems like a simple task. You choose an amplifier with a bandwidth that is appropriate for the input-signal requirements, then connect the amplifier directly to the ADC as a buffer. Not so fast. You are not finished until you accommodate the effects of the ADC-input charge injection on your amplifier (Figure 1). The transient currents at the input of the SAR ADC can disrupt the output of the amplifier so that the conversion process produces inaccurate digital results.

You model the input structure of the SAR ADC with a switch to an input capacitor,  $C_{SH}$ , to ground (Figure 2). Prior to signal acquisition, the ADC  $S_2$  switch connects the power supply, voltage reference, or ground to precharge  $C_{SH}$ . Your particular ADC topology determines this pre-

charged voltage value. At the start of the signal-acquisition time,  $S_2$  opens and  $S_1$  closes. When  $S_1$  closes, the system injects charge onto or off of  $C_{SH}$ , and the ADC takes a predetermined amount of time to acquire the signal. During this signal-acquisition time, the ADC requires ample charge from an input source to bring the system within a 1/2-LSB accuracy window.

To design your circuit to perform accurately with the first pass, insert a resistor,  $R_{IN}$ , and a capacitor,  $C_{IN}$ , in the signal path between the amplifier and the ADC (Figure 2). The capacitor serves as a charge reservoir providing ample charge to the input capacitor of the ADC.  $R_{IN}$  isolates the amplifier from  $C_{IN}$  and stabilizes the amplifier (Reference 2). The combination of  $R_{IN}$  and  $C_{IN}$  at least needs to meet the ADC's acquisition time (Reference 3). Finally, select your amplifier bandwidth to match the  $R_{IN}C_{IN}$  time constant.

If you design your SAR-ADC circuit by simply driving the input of the converter with an amplifier, it may not produce good results. If you insert an RC pair between the amplifier and the SAR ADC, you will successfully charge your converter and design the quirks out of your circuit from the start. EDN

## REFERENCES

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- 2 Green, Tim, "Operational Amplifier Stability, Part 3 of 15:  $R_O$  and  $R_{OUT}$ ," *Analog Zone*, 2005, [www.analogzone.com/acqt0307.pdf](http://www.analogzone.com/acqt0307.pdf).
- 3 Oljaca, Miro, and Bonnie Baker, "Start with the right op amp when driving SAR ADCs," *EDN*, Oct 16, 2008, [www.edn.com/article/CA6602451](http://www.edn.com/article/CA6602451).

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