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Physical design and architectural design

Historically, in the semiconductor-design flow, tapeout came after the last stages of the physical-design creation and verification. It was the final step before the design entered the manufacturing process, and it typically occupied less than 20% of the project-development schedule. Generally, a group other than the design team performed the tapeout and used separate design tools to construct a manufacturable view of the design. This division of labor no longer holds true.

Most of today's big digital ICs are actually SOCs (systems on chips). As a result, the engineering-design team has to stay involved through both

the block design and the physical design. The shift in physical-design tools to incorporating gate and sizing changes you base on physical-synthesis and -optimization tools now requires the involvement of engineering-design personnel through tapeout, as well. Issues that are now part of the physical-design flow include gate sizing, logic changes and optimization, buffer insertion, split-path creation, signal integrity and shielding, and IR-drop analysis. The analysis of these issues requires both the physical-design team and the block-design team.

The proliferation of deep-submicron processes has also led to an expanded tapeout scope, which now encompasses architectural design. Tapeout must address design trade-offs, such as power, I/O structures, memory structures, display interfaces, and programmability.

The power trade-offs include power-reduction methodologies, such as multithreshold CMOS, gated power, and multiple options for threshold

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voltage. These factors affect the overall physical-design floorplan and global routing constraints. Further, modern I/Os often require multiple power rings, also strongly impacting tapeout. These power rings usually offer minimal documentation, include complex interconnect, and require specific placement criteria.

Memory structures are typically hard macros, which means that the memory instance appears in the final chip as a placement of a complete memory block that the designers have neither edited nor modified. A third-party IP (intellectual-property) provider or a memory-compiler program—not the chip designers—creates the memo-

ry block. Such blocks are architectural elements for the tapeout team because the clustered or distributed nature of the memories and their internal organization impact the data buses and block locations in the chip.

Display interfaces are relatively new functions that both impact the tapeout flow and have architectural and block-design aspects. Historically, chips used private display interfaces connected to discrete LEDs, simple LED/LCD panels with segments and icons, or custom icon displays you could toggle that basically were printed versions of standard displays. But software configures and drives most modern displays, and the displays connect to the SOC through a standards-based interface. As a result, the timing of these interface blocks and the clustering of the I/Os for these blocks—a display port, for example—impose guidelines on tapeout teams' plans for physical placement.

As with the displays, there is a major trend in control logic toward embedding standard functions, such as microcontrollers, into designs and using external memory to program the functions. This practice minimizes the number of critical-path circuits in the design but locks much of the physical design into fixed macros. The physical-design tools behave differently with high block granularity—lots of small cells—than they do with high block obstruction—lots of big, immovable blocks with fixed pin locations. As a result, this facet of the architectural design also directly affects the number and type of tapeout-design trade-offs an SOC requires. **EDN**

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