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READERS SOLVE DESIGN PROBLEMS

Digitally programmable-gain amplifier uses divergent-exponential curve

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DPGAs (digitally programmable-gain amplifiers) are handy signal-processing components whenever ADCs must acquire signals with a wide dynamic range. Without the

ability to accommodate input-signal amplitude to match and efficiently use ADC span, low-level inputs may not be digitized with adequate resolution, and high-level inputs may overrange

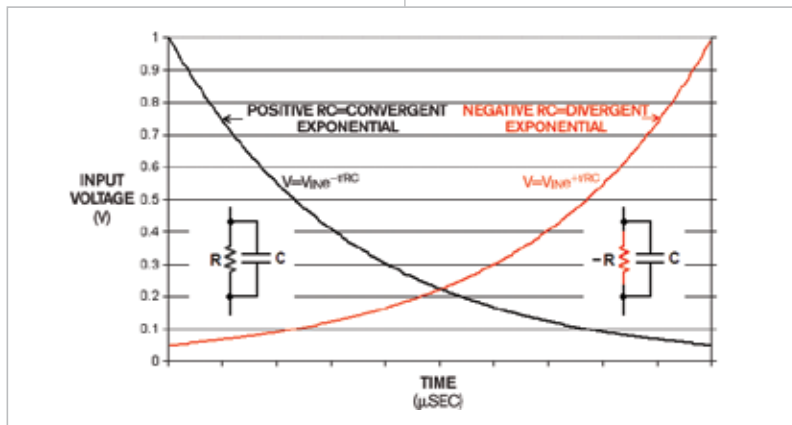


Figure 1 The behavior of the RC topology is still simple when you replace R with an active circuit that synthesizes a negative resistance.

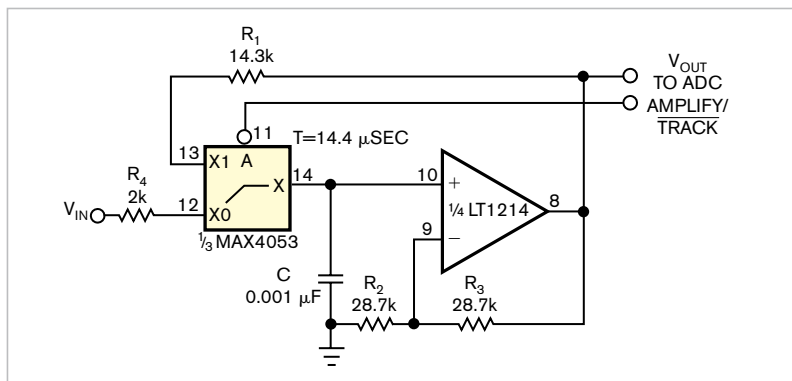


Figure 2 The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology.

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the ADC and be lost altogether.

Currently available DPGA designs typically incorporate a multiplying DAC into an op-amp-feedback loop, so that the input code to the multiplying DAC sets the amplifier's closed-loop gain. Several available monolithic DPGAs, such as Linear Technology's (www.linear.com) LTC6910 and National Semiconductor's (www.national.com) LMP8100, employ this topology. But the DPGA's digital-gain-control bits are sometimes inconvenient to provide, and these devices' output span may be inadequate, for example, to interface to $\pm 10\text{V}$ ADC-input spans. Also, the resolution of these devices' available gain settings is usually coarse—for example, 2-to-1 per gain step—and their power consumption is sometimes large. In contrast, this Design Idea describes a new DPGA that employs the concept of the divergent-exponential curve.

No waveform is simpler or more familiar than the $e^{-t/RC}$ -convergent exponential—the asymptotic discharge to zero of an elementary RC circuit initially charged to the input voltage, V_{IN} , in which $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V_{IN}/4$ at $t=2T$,

$V_{IN}/8$ at $3T$, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). Replacing R with $-R$ makes the RC time constant negative: $-RC$ and the waveform function yield the divergent exponential, $V_{IN} \times e^{+t/RC}$. Then, instead of converging to zero, the waveform diverges theoretically to infinity, and $V=2V_{IN}$ at $t=T$, $4V_{IN}$ at $2T$, $8V_{IN}$ at $3T$, and so forth. Therefore, no matter how small the input voltage might be, you can amplify it as much as you desire to any voltage by simply waiting the right amount of time $t = \log_2(V/V_{IN})T$ after starting the negative discharge.

The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology (**Figure 2**). When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant: $-(R_1 + R_{ON})(C + C_{STRAY}) = -14.4 \mu\text{sec}$, where R_{ON} is the on-resistance of the CMOS switch, and C_{STRAY} is the parasitic capacitance surrounding C (**Figure 3**). It also creates a diverging exponential: $V_{OUT}(t) = V_{IN} \times 2^{(t/10 \mu\text{sec} + 1)}$. Thus, $\text{gain} = 2^{(t/10 \mu\text{sec} + 1)}$. The 1- μsec timing resolution in the amplify-control bit provides 1.07-to-1 = 0.6 dB = 33 steps/decade gain-programming resolution. **Figure 4** graphs the voltage gain versus the time elapsed since the track/amplify-logic transition.

Unlike monolithic PGAs, DENT uses discrete components, such as op

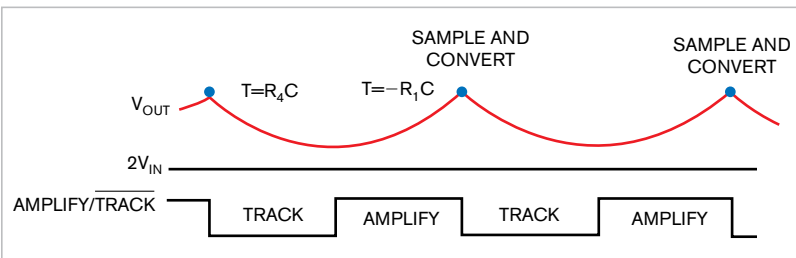


Figure 3 When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant.

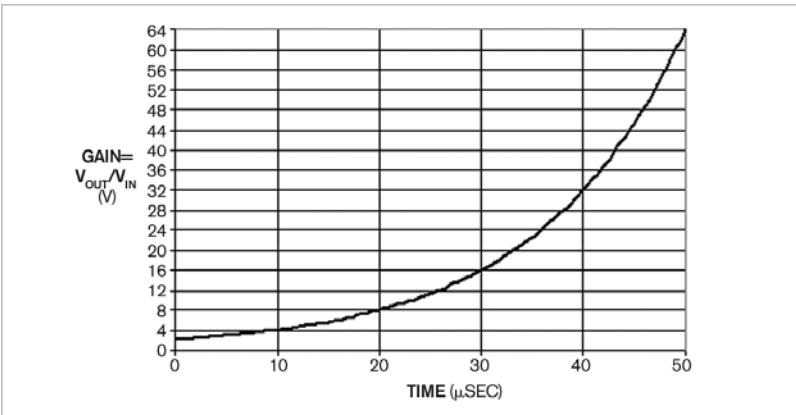



Figure 4 This graph shows the voltage gain versus the time elapsed since the track/amplify-logic transition.

amps and switches, so it can easily accommodate parameters such as I/O-voltage spans—negative inputs and 10V amplitudes—by choosing appropriate parts and power supplies. The accuracy and repeatability of the timing of exponential generation, ADC sampling, and RC-time-constant stability limit the practical performance of the amplifier in gain-programming accuracy and jitter. In the sample circuit, with $T=14.4 \mu\text{sec}$, 1 nsec of amplify-timing error or jitter equates to

0.007% of gain-programming error. Fortunately, the near ubiquity of programmable timer/counter hardware in popular microcontroller and data-acquisition peripherals usually makes the digital generation of a precisely repeatable amplify/track control an easy matter. On the analog side, possibilities exist for self-calibration algorithms that preserve gain-setting accuracy and relax RC-component-precision requirements, but they lie beyond the scope of this Design Idea. **EDN**

Circuit indicates ac-mains-fuse failure

By Vladimir Oleynik, Moscow, Russia

 Fuses are essential parts of power-distribution systems because they prevent fire or damage to electronic equipment. Fuses have the disadvantage of requiring replacement after every burnout, but they have the advantages of being inexpensive and

widely available. It is difficult to determine the failure time of fuses with ceramic or sand-filled bodies to prevent arcing. This Design Idea presents a simple circuit that solves this problem (**Figure 1**). It visually and audibly indicates ac-mains-fuse failure; in most

cases, audible indication is sufficient. The circuit works with a range of loads, and you can change its components to adapt to particular ac mains and load specifications.

When a fuse is in good order, the indication circuit is off because the fuse shunts it. When a fuse burns out, the indication circuit starts working. Capacitor C_1 reduces the ac-mains volt-

age, and bridge diode D_1 rectifies the ac voltage. Resistor R_1 limits inrush current when capacitor C_1 is discharged. Zener diode D_2 and capacitor C_2 form a dc voltage to operate a buzzer- and blinking-LED network. The blinking LED flashes, and buzzer B_1 , which has a built-in generator, sounds.

Like most other simple circuits, this circuit also has a disadvantage: It is incompatible with some load-power and ac-mains-voltage values. When a fuse burns out, the load stays connected to the ac mains, and the ac voltage divides between the circuit and the load. When the load is highly resistive or the ac-mains voltage is 110V rather than 220V, the circuit's operating voltage may be too low to drive the circuit. In that case, decrease the value of capacitor C_1 to 47 or 68 nF, after which the circuit's resistance rises. With the com-

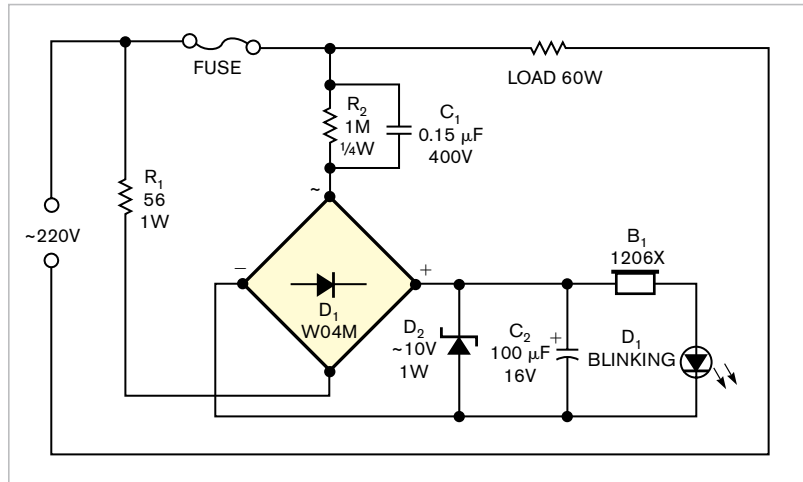


Figure 1 This circuit visually and audibly indicates ac-mains-fuse failure.

ponent values in **Figure 1**, the tested circuit operated with resistive loads of 20 to 200W. With higher-power loads,

the circuit operates well because, with higher load-power values, the circuit's load resistance is lower. **EDN**

Isolation MOSFET-driver IC gets improved power efficiency at lighter loads

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Many modern power MOSFETs reach low values of on-resistance at 5V even when the gate-to-source voltage is 5V. For heavy-duty power MOSFETs and, especially, IGBTs (insulated-gate bipolar transistors), however, engineers prefer gate-to-source voltages of 12 to 15V because the on-resistance of those power switches further decreases at higher gate-to-source voltages. The 17A-rated IRFR024 power MOSFET from International Rectifier (www.irf.com), for example, has an on-resistance of 0.075Ω (**Reference 1**). When the gate-to-source voltage is 12V, the device's on-resistance drops to 41% of its value compared to a case of a gate-to-source voltage of 5V. At a switching current of 10A, the device dissipates 6W less when the gate-to-source voltage is 12V.

IC_1 , an Analog Devices (www.analog.com) ADuM5230 IC isolation driver, can boost a 5V input to a level that's high enough to drive a MOSFET's on-

resistance to a low value, minimizing power dissipation (**Figure 1**). At low switching frequencies, however, the IC's high-side, internal 18V clamping dissipates the energy that the IC draws from the low-side 5V supply (**Reference 2**).

The ADuM5230's output is, however, unregulated. Fortunately, this IC has an adjustment pin that you can use to control the duty cycle of the device's internal PWM (pulse-width modulator) to reduce the duty cycle from a value of 1 to approximately 0.1. The default duty cycle has the value of 0.55 when the adjust pin is open. The lowest value of duty cycle occurs when connecting the adjust pin to the 5V supply. IC_2 , an ASSR-1219 advanced photo-MOSFET device from Avago Technologies (www.avagotech.com), controls the voltage at the adjust pin. The photo-MOSFET has 0V saturation voltage between its output terminals. As a classical optocoupler has

a bipolar phototransistor, using it as IC_2 would be less suitable in this case. A bipolar phototransistor has a saturation voltage of 0.4V, and, further, the CTR (current-transfer ratio) of a common optocoupler would decrease significantly when operating close to output saturation. Pulling the voltage at the adjustment pin to the external voltage-supply level comes into account when the high-side output of IC_1 has light or negligible loading.

At some point, V_{ISO} , the high-side output voltage of IC_1 , will exceed the value of approximately $V_Z(I_F) + V_{FLED} \sim 13.5V$, where $V_Z(I_F)$ is the voltage of zener diode D_1 at I_F , the forward current of D_2 , and V_{FLED} is the minimum forward voltage at D_2 , the LED of IC_2 . IC_1 exceeds this value, current starts to flow through the D_2 , and the MOSFET at the output of IC_2 becomes conductive. The manufacturer of IC_2 designed it for on/off operation and recommends a forward current of at least 0.5 mA (**Reference 3**).

At signal-level loading of the MOSFET at the output of IC_2 , a few tens of microamperes of forward current through the LED cause the photo-MOSFET's on-resistance to change

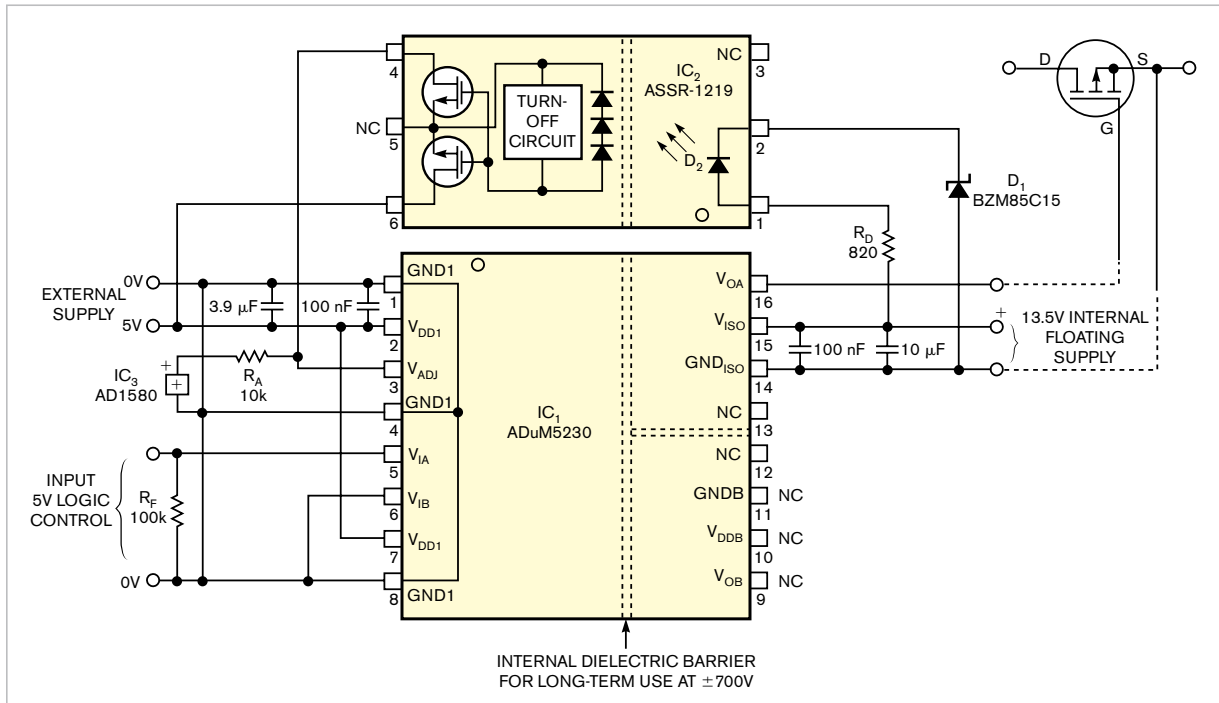


Figure 1 Connecting optical feedback by opto-MOSFET IC₂ in the power-MOSFET-driver IC₁ stabilizes the high-side output voltage to 13.5V at values of loading current down to 3.7 mA. The power efficiency of the circuit increases for a loading current of less than 7 mA.

from an almost-infinite value to a value of kilohms. The voltage level at the adjust pin then increases, and the duty factor of both the PWM in IC₁ decreases. This action establishes an isolated negative-voltage feedback. Thus, the temperatures of both the MOSFET and the LED in IC₂ have little effect on the properties of the circuit. At lighter loads, the current drain of the 5V supply is much lower than that of IC₁ with its adjust pin open.

Under test, the default supply current of the unloaded IC₁ was approximately 94.6 mA. This value decreases to 31.7 mA with the feedback in the circuit.

At heavy loading, the high-side output current of IC₁ rises to approximately 20 mA, and the duty factor rises automatically to a proper value that's higher than at the default supply current. Thus, the output voltage is roughly 13.5V within the range of approximately 3.7 to 22.6 mA. The power efficiency of the circuit is 20% or greater. At an output current of 4.5 mA, the power efficiency is 20.5%, and the power efficiency for IC₁ is approximately 15%. At a current of 3.7 mA, the circuit reaches 20% efficiency, a value that's considerably higher than the 13% in IC₁ with its adjust pin open. **EDN**

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Synthesize variable resistors with hyperbolic taper

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In adjustable, frequency-selective RC networks, the reciprocal of an RC product, $\omega_c = 1/RC$, determines the corner frequencies of the

network. If the adjustable elements are potentiometers with a linear-control characteristic—that is, taper— $R(\alpha) = \alpha R_p$, where α is the normalized

wiper position, $0 \leq \alpha \leq 1$, and R_p is the potentiometer's end-to-end resistance, then the corner frequencies are reciprocal functions of the potentiometer's wiper position, and the frequency scale compresses at the high end of the adjustment range. This situation is usually undesirable because it complicates adjustment of the network at the high

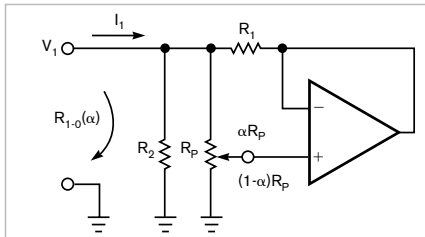


Figure 1 This simple circuit synthesizes a grounded variable resistance with a hyperbolic-control characteristic.

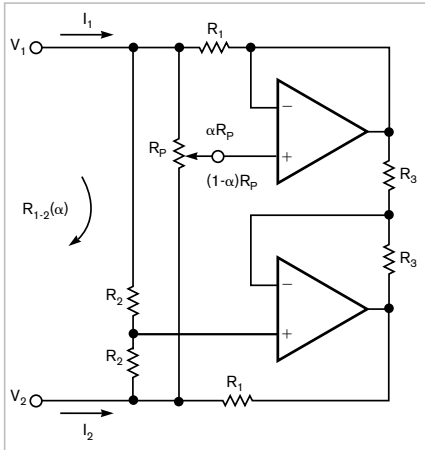


Figure 2 You can realize a floating variable resistance, with hyperbolic taper, with this circuit. Note that fixed resistors with the same number are matched pairs.

end. To make the frequency scale linear requires a control element with a hyperbolic taper—that is, something in the form $R(\alpha) = R_p / (A + \alpha B)$. Such variable resistances are not generally available from manufacturers, but you can synthesize them using a lin-

ear taper potentiometer and a few other components.

Figure 1 shows a simple circuit for producing a ground-referenced variable resistance having the desired hyperbolic-control characteristic. Analysis of this circuit yields the following relationship between the control setting and the resistance from Node 1 to ground: $R_{1-0}(\alpha) = R_1 R_2 R_p / (R_1 R_2 + R_1 R_p + \alpha R_2 R_p)$, $0 \leq \alpha \leq 1$. If you use this resistance in series or in parallel with a capacitor, the resulting corner frequency will be a linear function of α : $\omega_C = (R_1 R_2 + R_1 R_p + \alpha R_2 R_p) / R_1 R_2 R_p C$. The minimum and maximum values for R_{1-0} are $R_{1-0MIN} = R_1 R_2 R_p / (R_1 R_2 + R_1 R_p + R_2 R_p)$ and $R_{1-0MAX} = R_2 R_p / (R_2 + R_p)$.

To design this circuit for specific values of R_{1-0MIN} and R_{1-0MAX} , choose $R_p > R_{1-0MAX}$, and then compute $R_1 = R_{1-0MAX} R_{1-0MIN} / (R_{1-0MAX} - R_{1-0MIN})$ and $R_2 = R_p R_{1-0MAX} / (R_p - R_{1-0MAX})$.

You can extend the basic circuit of **Figure 1** to produce a floating variable resistance with hyperbolic taper (**Figure 2**). The value of the floating resistance between nodes 1 and 2 is $R_{1-2}(\alpha) = 2R_1 R_2 R_p / (2R_1 R_2 + R_1 R_p + 2\alpha R_2 R_p)$, $0 \leq \alpha \leq 1$, and the minimum and maximum values for R_{1-2} are $R_{1-2MIN} = 2R_1 R_2 R_p / (2R_1 R_2 + R_1 R_p + 2R_2 R_p)$ and $R_{1-2MAX} = 2R_2 R_p / (2R_2 + R_p)$. To design the circuit of **Figure 2** for specific values of

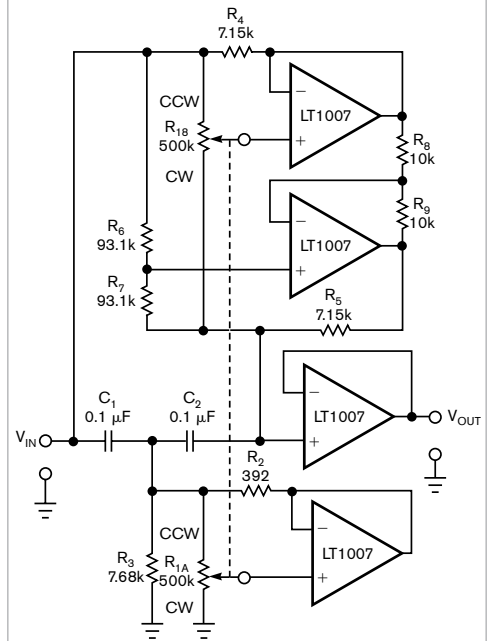


Figure 3 The basic circuits of figures 1 and 2 have been used in the design of a bridged-T notch filter with a variable notch center frequency and a linear frequency scale.

R_{1-2MIN} and R_{1-2MAX} , choose $R_p > R_{1-2MAX}$ and then compute $R_1 = R_{1-2MAX} R_{1-2MIN} / (R_{1-2MAX} - R_{1-2MIN})$ and $R_2 = \frac{1}{2} R_p R_{1-2MAX} / (R_p - R_{1-2MAX})$. Note that the value of the R_3 resistors does not directly affect the value of $R_{1-2}(\alpha)$. You should choose resistors that are large enough to not excessively load the op-amp outputs.

Figure 3 illustrates the application of the circuits in **figures 1** and **2** to the design of an adjustable bridged-T notch filter with a linear frequency scale. The filter has a notch center frequency that is adjustable from 50 to 1000 Hz and a notch depth of -20 dB. These requirements and the choice of 0.1- μ F capacitors for C_1 and C_2 dictate that R_{1-0} varies from 375 to 7503 Ω and that R_{1-2} varies from 6752 to 135,047 Ω . (A side benefit of using this technique is that it frees the designer from the restrictions of the limited number of standard end-to-end resistance values that potentiometer manufacturers offer.)

Figure 4 plots the Spice-simulated notch center frequency for the circuit of **Figure 3** against the normalized wiper position. The notch center frequency is a linear function of the control position. **EDN**

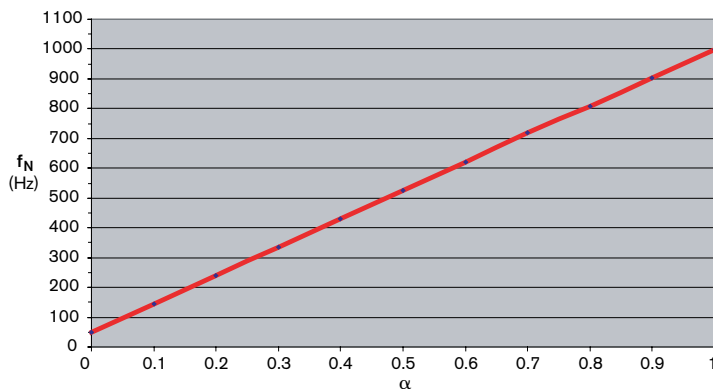


Figure 4 The Spice-simulated notch center frequency for the circuit of **Figure 3** versus the normalized wiper position shows that the notch center frequency is a linear function of the control position.