

SIMULATION GETS SPEED, CAPACITY BOOST

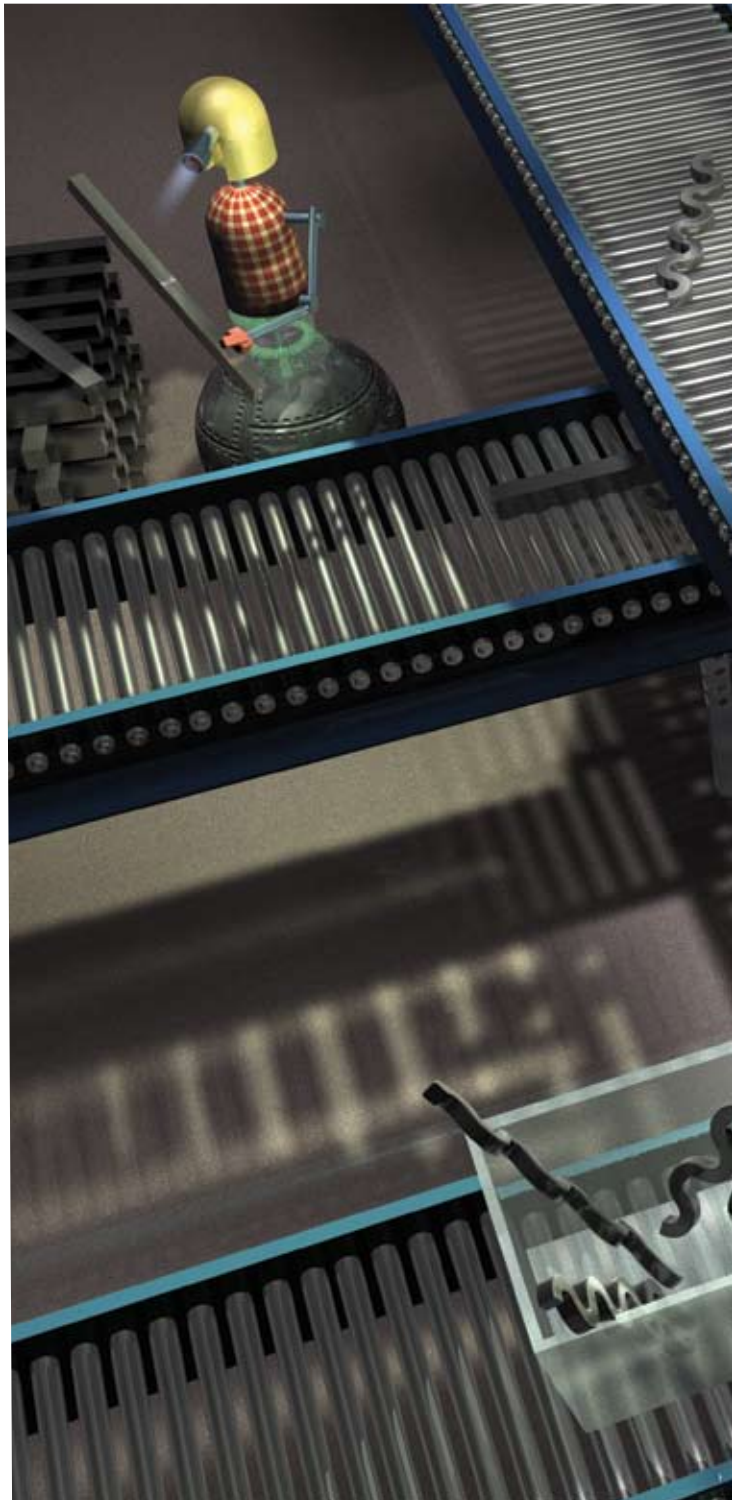
BY RICK NELSON • EDITOR-IN-CHIEF

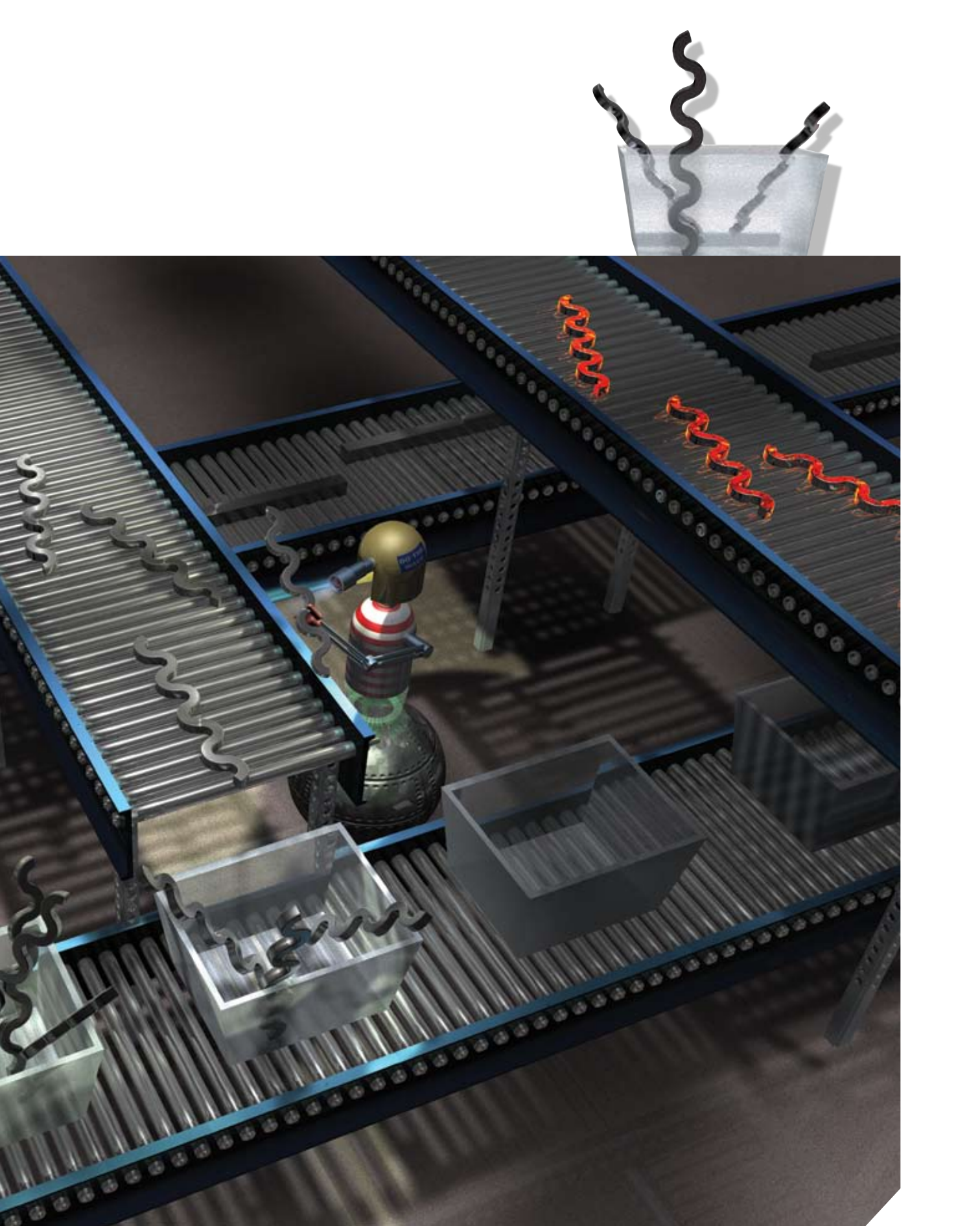
ANALOG- AND RF-SIMULATION TOOLS OFFER CHOICES OF SIMULATION SPEEDS AND SUPPORT HIERARCHICAL DESIGN STRATEGIES.

Speed, accuracy, and ease of use are key demands of designers employing simulation to get their analog-, RF-, and mixed-signal devices to market. Flavors of the venerable Spice simulator remain the tools of choice for analog simulation, and EDA vendors are enhancing the speed and accuracy of their tools through innovative techniques, such as adapting them to run on multicore processors or multi-CPU systems. Other companies are rewriting core Spice algorithms to speed simulations. Still others are focusing on top-down designs.

But Spice remains only part of the simulation picture as designers add RF/wireless-communications capability to an increasing array of products. And even products that offer no RF/wireless features are exhibiting RF performance as process geometries shrink, digital speeds increase, and high-speed serial-I/O ports proliferate. Furthermore, in many cases, as frequencies rise and designers squeeze more functions into smaller and smaller spaces, chip and board design cannot occur in isolation; co-design and simulation of chip, chip package, and board must take place.

How-Siang Yap, a member of the EDA-product-marketing group at Agilent Technologies' EEsof division, outlines the cross-domain-simulation technologies that can contribute to an effective co-simulation approach. First, he says, you need nu-





meric-domain tools, such as The MathWorks' Matlab or Agilent's Ptolemy, as well as C++, System-C, and standard HDLs (hardware-description languages). You also need frequency-domain ac-simulation tools that can work with S parameters and implement harmonic-balance techniques. For the time domain, Yap adds, you need Spice tools. Before committing your design to hardware, he advises, you should employ EM (electromagnetic)-domain tools that can apply method-of-moment and finite-element-analysis techniques to troubleshoot proximity and transition effects.

SPEEDING UP SPICE

As for Spice itself, efforts center on improving speed without compromising accuracy. Addressing this issue, Cadence Design Systems last month announced the availability of the Cadence Virtuoso APS (Accelerated Parallel Simulator), its next-generation circuit simulator, which constitutes a part of the Ca-

AT A GLANCE

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dence MMSIM (multimode-simulation) 7.1 release. John Pierce, senior architect at Cadence, says that the new simulator reduces mixed-signal-simulation turn-around time from days or weeks to a few hours. According to Nebabie Kebebew, a senior product manager at Cadence, the new simulator provides significant single-thread and scalable-multithread performance boosts and maintains accuracy equivalent to that of the Cadence Virtuoso Spectre circuit simulator. Kebebew says that more than 20 beta customers have tested the new simulator on more than 200 designs for devices including PLLs (phase-locked loops), DACs, ADCs, memory, power-management circuits, and high-speed I/O circuits. One customer, she says, experienced a 60-fold performance speedup for the simulation of a 65-nm PLL design running on an eight-core system. Another, she adds, experienced 58-times-better performance for the postlayout simulation of a dc/dc converter, reduc-

EM SIMULATION: FROM PCBs TO HELICOPTERS

As products become more complex and operate at higher frequencies, it's increasingly important to investigate signal- and power-integrity issues to simulate EMC (electromagnetic-compatibility) and EMI (electromagnetic-interference) effects. Tools that can help include CST's (Computer Simulation Technology's) PCB (printed-circuit-board) Studio, which supports 2- and 3-D simulations and can determine skin effect in the time and the frequency domains. It can import IBIS (I/O-buffer-information-specification) models and interfaces Spice-equivalent tools. With the CST Cable Studio, it supports co-simulation of PCBs and attached cables.

The company integrates PCB Studio and Cable Studio within Studio Suite 2009 EM-simulation software, which enhances design throughput by automating optimization and by applying the most appropriate solver technology to a given problem (Figure A). Studio Suite 2009 supports transient-EM and circuit co-simulation, and it offers a 64-bit front end plus MPI (mes-

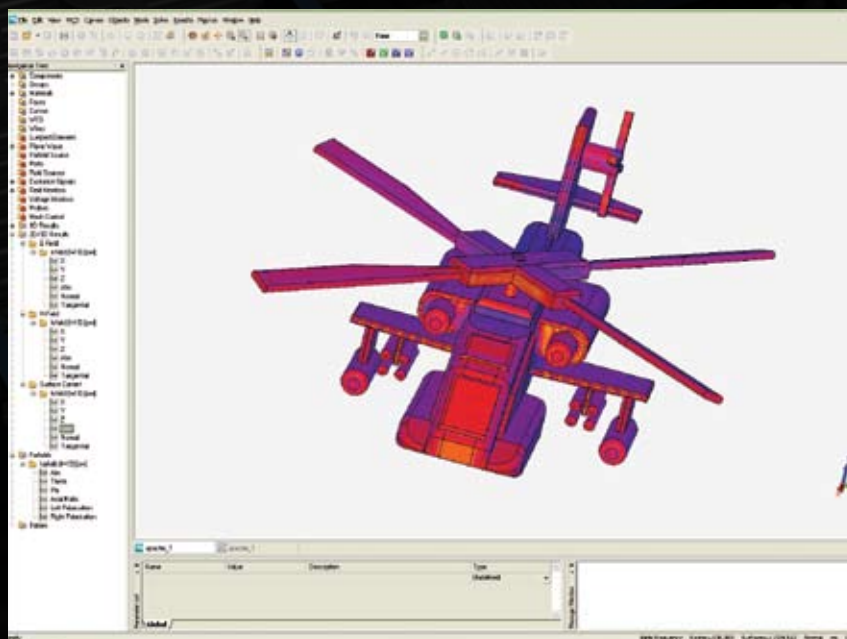


Figure A CST Studio Suite 2009 generated this simulation of the EM fields on the surface of an Apache helicopter to 10 GHz.

sage-passing-interface)-based parallelization to speed the simulations of large and complex structures. It includes a transient thermal solver

to simulate heating processes and employs a bioheat equation for realistic modeling of physiological cooling effects.

ing runtime from 20 hours and 16 minutes to 21 minutes.

Mentor Graphics has also been working to speed simulation. The company in October introduced a new version of the Eldo and Eldo RF transistor-level analog simulator, which improves raw-speed performance without compromising accuracy. The new version employs a revised matrix-solving strategy as well as a scalable multithreading technology that allows users to take advantage of inexpensive multi-CPU hardware.

According to Tony Liao, Mentor's deep-submicron-business-development manager, the multithreaded Eldo can run from three to 10 times or more faster than the single-core version, depending on the number of active devices and parasitic elements in a circuit. For faster simulation, he says, customers can employ the ADiT fast-Spice simulator, although at the cost of some accuracy. An ADiT-to-Eldo interface permits a circuit to run with both simulators; portions that require high accuracy run on Eldo, and the other portions run on ADiT. Liao notes that the simulators support co-verification through their links to Mentor's ModelSim digital simulator. The simulators' links to Mentor's ICAlyst help support design verification. In addition, the simulators work together within Mentor's ADMS (Advance mixed-signal) simulator environment (Figure 1).

Synopsys, too, has worked on speeding Spice and has announced improvements to its HSpice core-engine technology as well as new multithreading capabilities in the March 2008 release of its HSpice simulator. According to Geoffrey Ying, director of marketing for mixed-signal-simulation products at Synopsys, the company is adapting all its tools to take advantage of multicore processors, with HSpice being the first

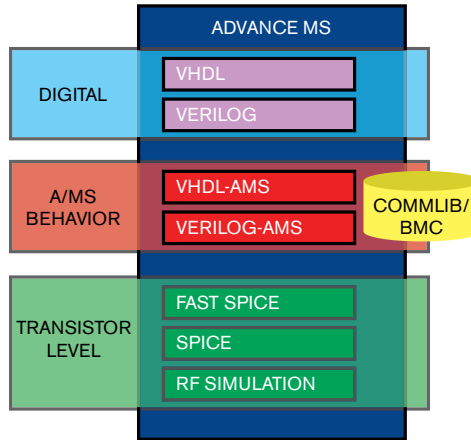


Figure 1 The ADMS (Advance mixed-signal) simulator from Mentor Graphics supports multiple modeling languages. The CommLib/BMC (behavioral-model-calibration) library contains parameterized analog- and mixed-signal models for communications applications.

to migrate. He says that, with the multithreaded version, circuit designers can now run HSpice postlayout simulations as much as three times faster on single-core processors and as much as six times faster on four-core processors. The single-core speedup stems from improvements in the symbolic-dc-operating-point-convergence algorithm, transient time-step control, netlist parsing, and model performance. For multicore processors, the release enables simulation of postlayout designs containing more than a million resistive and capacitive parasitic effects.

Synopsys has worked with TSMC (Taiwan Semiconductor Manufacturing Co) on the TMI (TSMC Modeling Interface) methodology, which consists of a protocol for integrating custom device models into Synopsys' HSpice, HSim, and NanoSim circuit simulators. The TMI methodology delivers an innovative and efficient device-modeling approach for TSMC's process technologies at 40-nm and smaller geometries. Ying says that the TMI method, on average,

improves simulation time and reduces memory usage by a factor of five and takes into account both mechanical-stress effects in silicon and layout dependencies that alter the characteristics of device instances based on their proximity to other devices.

Magma Design Automation uses multiple CPUs instead of multiple cores and multithreading. The company's FineSim Spice leverages Magma's NPT (native parallel technology) to enhance speed and capacity and maintain accuracy by distributing computing load over multiple computers, according to KT Moore, Magma's senior director of business development for the custom-design-business unit. The approach "enables customers to simulate hundreds of thousands of devices on practical numbers of computers—eight, not 100," he says.

Despite the performance increases of multithreaded and multicomputer implementations of Spice, a need for fast-Spice implementations will continue. "In different phases of a design process, the requirement for accuracy changes," Moore says. "Early on, you are more focused on functionality. As you narrow down your design to focus on the actual operating points and characteristics, then you want to tighten up the accuracy. A lot of large designs have millions of transistors; you could simulate [those transistors] using our Spice engine running on multiple CPUs, and that [approach] might be great for a sign-off simulation." He claims, however, that for regression or functional simulation, NPT is the tool you would probably want to use.

Traditional EDA companies are getting competition in the Spice arena from relative newcomers that at times blur the line between true Spice and fast Spice. For example, fast-Spice tools tend to trade accuracy for speed, says Paul Estrada, chief operating officer at Berkeley Design Automation. However, manufacturers often market these fast-Spice tools with a "Spice-accurate" label. Berkeley Design Automation's Analog Fast Spice, he claims, truly does provide fast-Spice capacity and performance with true Spice accuracy. The tool does no approximations, Estrada says. In-

TABLE 1 RELATIVE PLL SIMULATION TIMES WITH SPICE AND VERILOG-A MODELS

Phase detector	Charge pump	VCO	Divide by N	Relative CPU time
Spice	Spice	Spice	Spice	100x
Verilog-A	Spice	Spice	Verilog-A	64x
Verilog-A	Spice	Verilog-A	Verilog-A	13x
Verilog-A	Verilog-A	Verilog-A	Verilog-A	1x



stead, it runs original device equations and solves the original full-circuit matrix, providing waveforms that are as good as or better than those of any other Spice engine.

Analog Fast Spice provides its performance improvements running on a single-core processor. Estrada attributes its performance levels to the fact that its developers need not attempt to optimize legacy code. “Look under the hood at any of today’s Spice engines,” he says, “and you’ll see that they are basically structured like a rat’s nest. Everything is interwoven with everything else, and, if you try to improve one area of the simulator, you invariably make another area worse.” Analog Fast Spice employs a modular architecture in which you can optimize each module without disturbing other modules. Looking to the future, the company is seeing good results with multithreading but hasn’t yet released a multithreaded version.

Gemini is also employing multithreading to improve performance. The company targets 95% of the Spice-accurate-tool and fast-MOS-Spice market, says Kent Jaeger, vice president of sales and marketing. The Gemini holistic multithreaded Spice, he says, provides two- to 10-times better performance without compromising accuracy. “We forbade [our designers] to use any technique that would potentially sacrifice Spice accuracy.” The Gemini simulator outperforms fast-MOS-Spice simulators in 90% of benchmark tests and runs on low-cost Intel multicore processors running the 64-bit Linux operating system.

Infinisim borrows some techniques from fast-Spice yet preserves Spice accuracy, according to the company’s chief technology officer, Zakir Syed. The company’s RASer (real-time-adaptive-simulation) simulator works at all stages of design verification—from single-block to full-chip and from prelayout to post-layout. According to Anand Iyer, senior director of marketing, RASer targets the critical need for doing total system simulation to avoid the need for silicon respins. “Traditional Spice simulators run out of steam after a few hundred thousand elements, and even with parallel processing, capacity cannot improve,” he says.

Fast-Spice-like approaches come in handy at this point. “We break up [a cir-

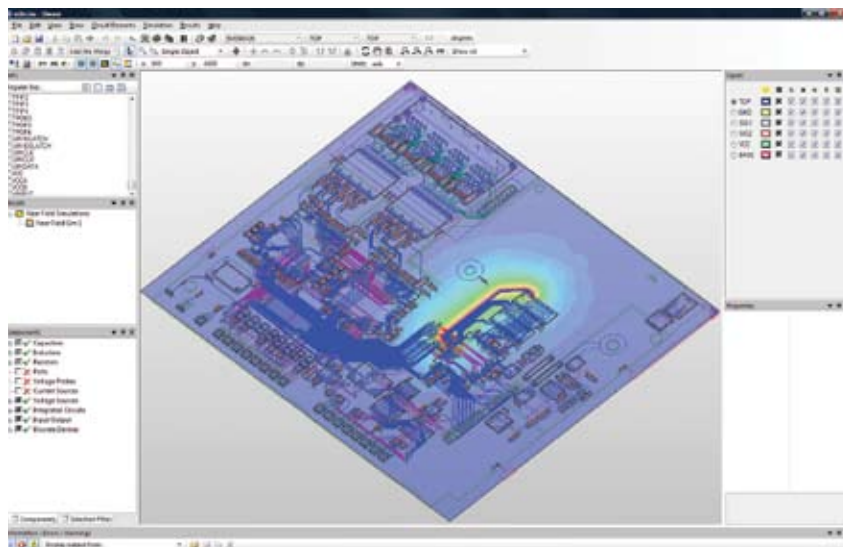


Figure 2 The SIwave tool can help identify and solve signal-integrity issues on PCBs (courtesy Ansoft).

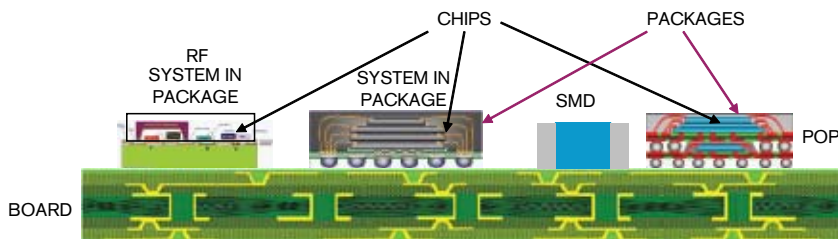


Figure 3 The efforts of consumer-product manufacturers to provide higher functional density at lower cost are resulting in the squeezing together of digital, analog, and RF functions into small volumes. That squeezing results in the need for chip, package, and board co-design using tools such as the Agilent EEsof ADS.

cuit], just as fast Spice would, into smaller partitions, and then we apply different solvers to different partitions,” says Syed. “In fast Spice, you lose accuracy, but ... we use the exact device models that Spice uses.”

Although Infinisim supports multithreading, the company focuses on speeding up individual threads. “Companies are developing multicore algorithms on Spice,” Syed says, “and ... these companies have given up on improving Spice.” He says that, in some cases, such as Monte Carlo simulation, multithreading and distributed computing apply. In those cases, any simulation is independent of the other simulations.

“In analog designs, [we see] iterations in which you typically run five corner models and temperature sweeps,” says Nicolas Williams, director of product management at Tanner EDA. “If you want to do Monte Carlo analysis, you

[must] run thousands of simulations on your one circuit. It’s easy to farm out those simulation runs from a single command deck.” It’s the simulation job level, not the circuit level, in which parallelization can offer the most benefits, he adds.

Tanner’s T-Spice simulator aims at the design of big-analog, small-digital chips. The company has integrated Verilog-A to support both simulations with behavioral models and device-level Spice models. Verilog-A supports top-down design and offers significant advantages over the bottom-up approach that analog designers traditionally employ. Williams says that top-down design can eliminate costly and time-consuming design iterations that can be necessary when a bottom-up approach results in system-integration problems that occur late in the design cycle.

He notes that analog designers em-



ploy behavioral-modeling techniques when, for example, they use dependent sources, and they may use The MathWorks' Matlab to calculate coefficients, but, until now, they have lacked a behavioral language within a Spice-programming environment. The combination of Spice and behavioral models allows designers to focus on block design and perform simulations without lengthy runtimes. **Table 1** shows the relative CPU times for simulating a PLL with its components represented in various combinations of Spice and Verilog-A models.

BEYOND SPICE

Even a thoroughly simulated and verified chip design has no guarantee that a device will work properly when real silicon meets the real world. Silicon performance succumbs to the EM effects of the chip package, the board the package is mounted on, or the large-scale structure containing the board (see **sidebar** "EM simulation: from PCBs to helicopters"). Larry Williams, director of business development at Ansoft, recounts the story of a semiconductor manufacturer whose device worked on an evaluation board with nicely separated traces and lots of power and ground planes to isolate signals. However, the device exhibited abnormal behavior when the manufacturer's customer crammed it into a tiny consumer product in which the traces were much closer together, causing more coupling. All of a sudden, the chip's radio began to misbehave, generating unacceptable out-of-band spurious responses. "We worked to show how to solve the problem by using a complete system-level simulation of the chip, the chip package, and board," says Williams. Ansoft used the manufacturer's Spice-level model for the IC and performed 3-D extractions to create models of the IC's BGA package and the PCB (printed-circuit board). "We coupled all three together in our environment, and, lo and behold, we could predict those spurs," he says.

Ansoft's offerings include HFSS (high-frequency simulator system), which performs 3-D electromagnetic-field simulation of high-frequency and high-speed components, and SIwave (signal-integrity wave), which allows engineers to extract frequency-dependent circuit

models of power-distribution and signal nets directly from device layout—that is, physical CAD (computer-aided-design)—databases to help identify signal-integrity and power-distribution problems (**Figure 2**). "The problems we solve are showstoppers," Williams says, adding that addressing SI is critical: "Companies are setting up SI departments to ensure reliable electronic

performance. Look at any modern handheld electronic device; it may have several radios with a lot of digital content to provide a rich user experience. It will operate at low voltage to conserve power, and digital signals will consequently be sensitive to coupling. We allow an engineering design team to read in a PCB model, couple that with IC-package-model extractions, and cascade all

those things together to perform an entire system-level simulation.”

EEsof's tools, including the ADS (Advanced Design System), had their origin with a group at Hewlett-Packard that developed RF and microwave instruments. ADS 1.0, which debuted in 2000, enabled designers to simulate RF circuitry along with digital circuits, including DSPs. The tool originally found extensive use

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in WLAN (wireless-local-area-network) designs and has continued to evolve. As manufacturers of consumer products strive to provide higher functional den-

sity at lower cost, they are squeezing together digital, analog, and RF functions into small volumes, creating a need for chip, package, and board co-design and simulation using ADS. EEsof's Yap cites two aspects of the co-design process: front end, which involves optimizing system partitioning for performance and cost, and back end, which deals with factors such as ball-pattern planning and routing plus I/O optimization.

A recent advance, he says, is support for nonlinear X parameters. Last month, Agilent announced that designers can generate X parameters either from simulation with ADS or from Agilent's test-and-measurement instruments to speed communications-product development. X parameters, says Yap, save significant amounts of time. With X parameters, a designer can acquire a model to use within a simulation. The alternative involves months of characterization and generates reams of plots that can be difficult to interpret.

As for the future, Yap sees continuing efforts to integrate electromagnetic simulation into the design flow to simulate everything from circuits to antennas. More products are going wireless, and, in compact products, the antenna is often on the PCB. The ability to identify potential problems before committing to hardware is critical, he says. **EDN**

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