

TABLE 1 RELATIVE PLL SIMULATION TIMES WITH
SPICE AND VERILOG-A MODELS

Phase detector	Charge pump	VCO	Divide by N	Relative CPU time
Spice	Spice	Spice	Spice	100x
Verilog-A	Spice	Spice	Verilog-A	64x
Verilog-A	Spice	Verilog-A	Verilog-A	13x
Verilog-A	Verilog-A	Verilog-A	Verilog-A	1x