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Increase the range of memorized voltage for a sample-and-hold device

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Sample-and-hold devices find use in front of ADCs. The basic sample-and-hold circuit comprises two op amps, A_1 and A_2 ; a switch, S_1 ; and a capacitor, C_1 (Figure 1). For many low-power op amps, the values of the input and output voltages can be only ± 10 to ± 14 V using a standard ± 15 V power supply. Enabling these devices

to handle greater voltage can significantly improve the resolution of an ADC.

You can increase the memorized voltage that amplifiers A_1 and A_2 can reach by using a variable power supply (references 1 and 2). This approach places additional voltage requirements on S_1 , however. To continue

using switches with the same range as the original, you must add two switches and independent control-logic blocks, CL_1 and CL_2 , for switches S_1 , S_2 , and S_3 (Figure 2). The

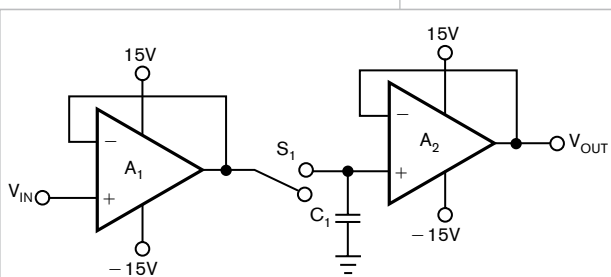


Figure 1 A basic sample-and-hold circuit comprises two op amps, a switch, and a capacitor.

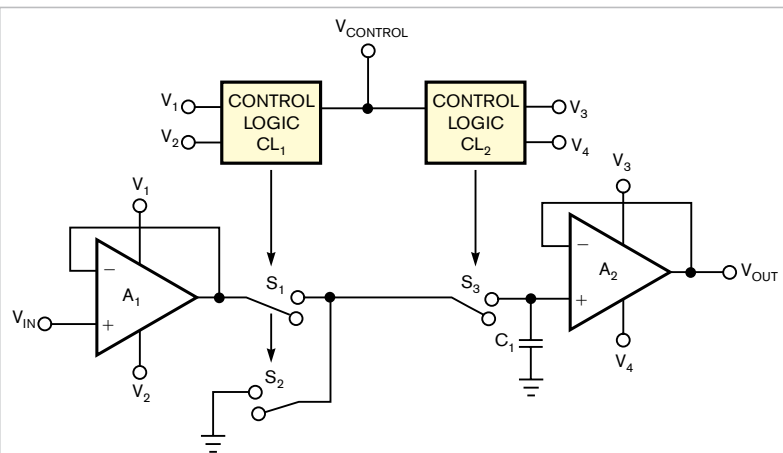


Figure 2 To continue using switches with the same voltage range as that of Figure 1, you must add two switches and two independent control-logic blocks.

DIs Inside

48 Inexpensive self-resetting circuit breaker requires few parts

54 Sinusoid generator uses dual-output current-controlled conveyors

56 Perform timing for micro-controllers without using timers

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two parts of the circuit may have independent power supplies. You apply the same variable voltages to amplifiers A_1 and A_2 as you do to control-logic blocks CL_1 and CL_2 , respectively. When S_1 and S_3 are closed, S_2 is open, and vice versa.

The resulting circuit keeps the voltages connected to the gate and substrate for the MOS transistors of each switch within the desired 30V range (Figure 3). (You derive this value from the sum of absolute-voltage values: $|V_1| + |V_2|$ and $|V_3| = |V_4|$.) Voltages V_1 and $-V_2$ connect to amplifier A_1 , control-logic block CL_1 , and the substrates of the transistors of switches S_1 and S_2 . Voltages V_3 and $-V_4$ connect to amplifier A_2 , control-logic block CL_2 , and the substrates of the transistors of switch S_3 .

You create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8 , which connect to the 30 and the -30 V power supplies and the output of amplifier follower A_1 (Figure 3). Transistors Q_1 and Q_2 create the change to the power supply of amplifier A_1 . Volt-

ages V_1 and V_2 also supply power to control-logic block CL_1 and the substrates of the transistors of switches S_1 and S_2 . CL_1 comprises transistors Q_{11} , Q_{12} , Q_{15} , and Q_{16} . It creates a control signal for gates Q_5 and Q_6 of switch S_1 and the inverse signal for gates Q_8 and Q_9 of S_2 .

Resistor dividers R_9 and R_{10} and R_{11} and R_{12} connect to the 30 and the $-30V$ power supplies, and the output of amplifier follower A_2 creates the

changing voltages V_3 and V_4 . Transistors Q_3 and Q_4 create the change to the power supply of amplifier A_2 . Voltages V_3 and V_4 also supply power to control-logic block CL_2 and the substrates of the transistors of switch S_3 . CL_2 is made up of transistors Q_{13} , Q_{14} , Q_{17} , and Q_{18} . It creates a control signal for gates Q_7 and Q_{10} of switch S_3 . Transistors Q_5 through Q_{10} and Q_{11} through Q_{18} of CL_1 and CL_2 , respectively, are complementary pairs of

MOS logic transistors. **EDN**

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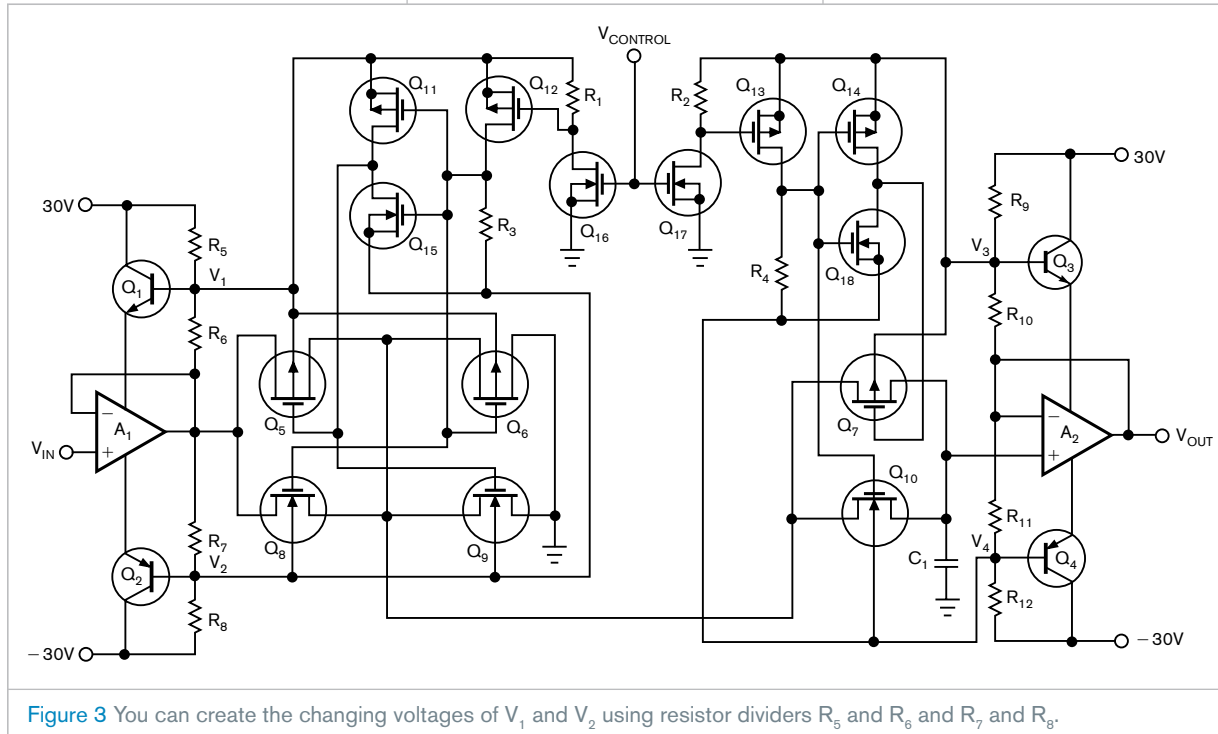


Figure 3 You can create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8 .

Inexpensive self-resetting circuit breaker requires few parts

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Most readers are familiar with the current-limiting circuit in **Figure 1**, in which the load current, I_L , is limited to a value of $I_L \approx V_{BE}/R_S$, where V_{BE} is the base-to-emitter voltage and R_S is the sense resistance. Under normal conditions, in which the base-to-emitter voltage is too small to bias Q_1 on, P-channel MOSFET Q_2 's gate resistor, R_G , biases Q_2 fully on, and

only the load resistance, R_L , and the load voltage, V_L , determine the load current. However, if the load current increases to a point at which the base-to-emitter voltage is approximately 0.7V, Q_1 starts to conduct and reduces Q_2 's gate-to-source voltage, V_{GS} , to a level that holds the load current roughly constant at a value you derive from $I_{L\text{MAXIMUM}} \approx 0.7V/R_S$.

This linear current limiter is effective for applications in which the maximum load current, the supply voltage, or both are relatively small. However, the power that the circuit's pass transistor, Q_2 , dissipates limits the circuit's applicability. For example, if the maximum load current is 200 mA and the supply voltage, V_S , is 24V, a short circuit across the load would dissipate almost 5W into Q_2 . Q_2 must handle this power with adequate margin, and additional heat-sinking may be necessary to keep its junction temperature at a safe level. Using larger values of

maximum load current, supply voltage, or both exacerbates this problem. In many applications, the cost, size, and weight of the components necessary to handle the short-circuit power dissipation may be prohibitive.

However, by adding a few inexpensive components, you can adapt the circuit to provide effective current limiting with none of the power-dissipation headaches. The resulting circuit functions as a self-resetting circuit breaker (**Figure 2a**). Again, Q_1 and R_S provide a current-monitoring function in which the sense voltage $V_{SENSE} = I_L \times R_S$. In this circuit, however, Q_2 is either fully on or fully off and never biases into its linear region. Because Q_1 's base current is normally small, the voltage drop across base resistor R_B is also small, such that the base-to-emitter voltage is approximately equal to the sense voltage.

To understand how the circuit works,

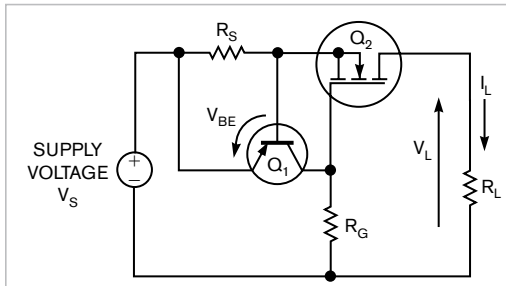


Figure 1 A conventional two-transistor current limiter prevents excessive current from reaching the load.

assume that the load current is initially low and the base-to-emitter voltage is less than 0.7V. Under these conditions, Q_1 is off and timing capacitor C_1 remains uncharged such that V_{IN} , the voltage at the input of Schmitt inverter IC_1 , is 0V. Thus, IC_1 's output is approximately 5V, biasing Q_3 on, which in turn provides gate bias for Q_2 through R_4 , allowing current to flow from the supply voltage into the load through the sense resistor and Q_2 's on-resistance.

If a fault now causes the load current to increase to a level at which the base-to-emitter voltage is approximately 0.7V, Q_1 turns on and its collector current rapidly charges C_1 . The input voltage now quickly rises toward the Schmitt inverter's upper threshold voltage, V_{TU} , at which point IC_1 's output goes low, turning off Q_3 and Q_2 . The load current now falls to 0A and the base-to-emitter voltage falls to 0V, thereby causing Q_1 to turn off. C_1 now begins to discharge through R_1

and R_2 , and the input voltage slowly falls toward the Schmitt inverter's lower threshold voltage, V_{TL} . At this point, IC_1 's output again goes high, Q_3 and Q_2 turn on, the circuit breaker resets itself, and the process repeats until you remove the fault.

The circuit's waveforms show the relationship between the input voltage and the load voltage (**Figure 2b**). Because load current flows into Q_2 only during the on-time, the average power it dissipates is directly proportional to the duty cycle: $P_{AVG} \propto t_{ON} / (t_{ON} + t_{OFF})$, where P_{AVG} is the average power in watts, t_{ON} is the on-time, and t_{OFF} is the off-time. Provided that C_1 , R_1 , and R_2 set a large enough time constant, the off-time will normally be much greater than the on-time, and the resulting power that Q_2 dissipates will be low. Like the linear-current limiter, the sense resistor sets the circuit breaker's current limit: $I_{LMAXIMUM} \approx 0.7V/R_S$ (A).

R_1 and R_2 form a potential divider that ensures that the input voltage can never exceed IC_1 's maximum input voltage. Select values such that the input voltage is 5V or less when Q_1 is fully on, where the voltage of C_1 is roughly equal to the supply voltage. Also, choose values that are large enough to provide a large time constant without requiring an excessively large value of C_1 . The selection of transistor Q_1 isn't critical, but you should select a device with good current gain and make sure that its maximum collector-to-emitter voltage is greater than the supply voltage. When choosing a P-channel MOSFET for Q_2 , re-

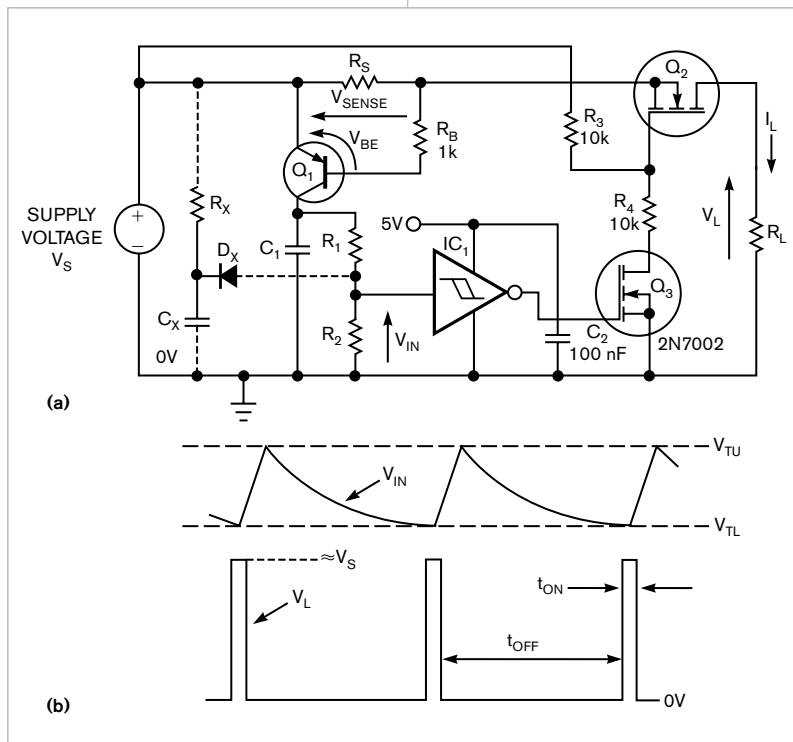


Figure 2 Adding a few components turns the current-limiting circuit into a pulser that reduces heat in the pass transistor, Q_2 (a). The circuit's waveforms show the relationship between the input voltage and the load voltage (b).

member that it must withstand the full supply voltage when you bias it off, so make sure that the maximum drain-to-source voltage is greater than the supply voltage. When choosing a value for the sense resistor, ensure that the base-to-emitter voltage is less than 0.5V at the maximum normal value of the load current.


Loads such as filament bulbs, ca-

pacitive loads, and motors that exhibit a large inrush current can cause the circuit breaker to trip on power-up. You can avoid these problems by adding capacitor C_X , diode D_X , and resistor R_X . On power-up, C_X is initially uncharged and pulls the input voltage toward 0V through D_X . This action prevents the circuit breaker from tripping until the inrush current

subsides. C_X and R_X determine a delay, after which the voltage on C_X eventually rises to the supply voltage, D_X becomes reverse biased, and the circuit breaker is then free to respond to overcurrent faults. Be prepared to experiment with the values of C_X and R_X to get the right delay time. Values of 10 μ F and 1 M Ω , respectively, are good starting points. **EDN**

Sinusoid generator uses dual-output current-controlled conveyors

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 Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption. Hence, designers employ several implementations of current mode in these devices for realizing various functions. A previous Design Idea introduced a second-generation dual-output current-controlled conveyor to create oscillators (**Reference 1**). Unfortunately, these circuits aren't available as ICs, but you build them from discrete components. **Figure 1** illustrates an active building block of such a circuit, which the following equations characterize: $I_Y=0$, $V_X=V_Y+I_XR_X$,

$I_{Z+}=I_X$, and $I_{Z-}=-I_X$. You can express the parasitic resistance at terminal X as $R_X=V_T/2I_B$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades. **Figure 2** shows the bipolar implementation of the circuit.

The circuit provides an extra degree of freedom in the sense that the control over the frequency of oscillation can be through both current and voltage. The circuit in the previous Design Idea provides various advantages, it this new circuit not only retains all those essential advantages, it also provides an extra feature of voltage controllability of frequency of oscillation.

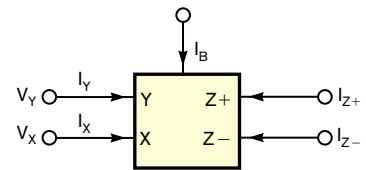


Figure 1 Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption.

Additionally, you can control the condition of oscillation using the conveyors' bias currents.

Figure 3 shows the proposed sinusoid-oscillator circuit. You can obtain the characteristic equation for the circuits as follows: $S_2C_1C_2R_{X1}R_{X2} + SC_2R_{X2} - SC_2R_{X1} + K=0$,

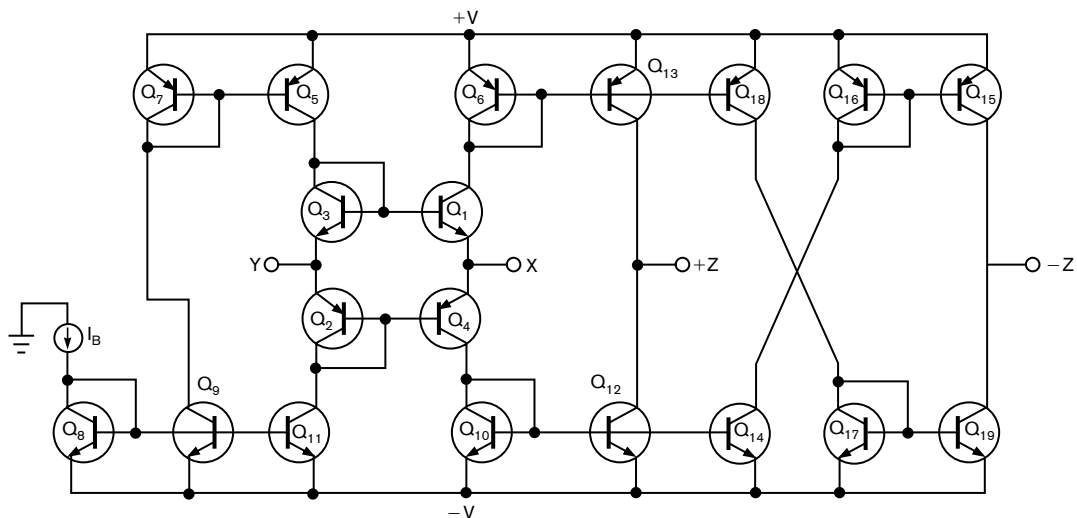


Figure 2 A current-controlled circuit uses no internal resistors or capacitors.

where K is the voltage multiplier. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360° —the required condition for oscillation is $R_{X1}=R_{X2}$, and the frequency of oscillation is $f=1/2\pi\sqrt{k/(C_1C_2R_{X1}R_{X2})}$.

Clearly, you can use the gain buffer to vary the frequency of oscillation, which is the area in which this circuit differs from the earlier Design Idea. You can use both current and voltage to control the voltage multiplier. The circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4} (Figure 4). For voltage control over K , you can use another circuit simply by using a noninverting op amp and replacing the resistors with MOSFETs working in that triode region. That approach simulates voltage-controlled resistors.

The circuit in Figure 2 underwent testing with a PR100N PNP transistor and an NPN NP100N transistor of the bipolar arrays ALA400 and a dc supply of $\pm 3V$ (Reference 2).

The circuit requires only two current-controlled conveyors, two grounded capacitors, and a voltage multiplier; it requires no floating capacitors and no external resistors, which makes the circuit's power consumption lower than that of RC oscillators. For a conventional bipolar-transconductance operational amplifier, the transconductance, g_m , is $I_B/2V_T$. Comparing

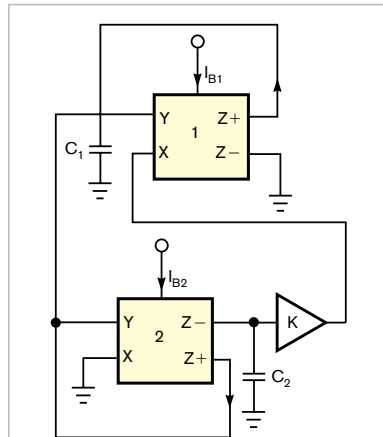


Figure 3 This configuration creates an oscillator from two current-controlled conveyor circuits.

this figure with the equivalent value of I_B , the transconductance of the bipolar-transconductance op amp is four times less than that of a dual-output current-controlled conveyor. Thus, the power consumption of the current-controlled-conveyor-based circuit is about four times less per active device than that of the op-amp-based circuit. The sensitivity study shows that $S_{K;R_{X1};R_{X2};C_1;C_2}^{\omega} = -1/2$; ω sensitivities are hence less than unity, which is an attractive feature of this circuit. Remember that creating an accurate oscillator model requires modeling equations to be nonlinear, and meeting the Barkhausen criteria is a necessary

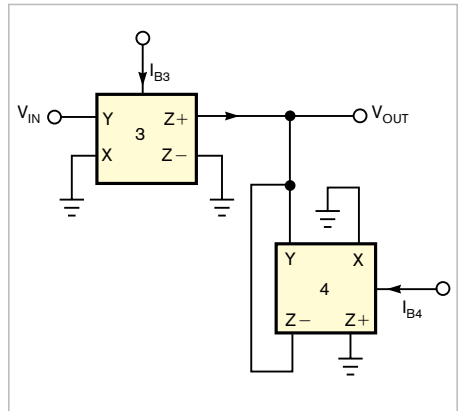


Figure 4 This circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4} .

condition for oscillation. Oscillator circuits may latch up and never oscillate even if you satisfy the Barkhausen criteria. **EDN**

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Perform timing for microcontrollers without using timers

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Microcontrollers now find use in every walk of life. Their peripherals vary from the general-purpose I/Os to the USB interface, making them versatile for a range of products. Timing is one key part of a typical microcontroller application. Low-cost microcontrollers have one or two built-in timers and often also have a watchdog timer.

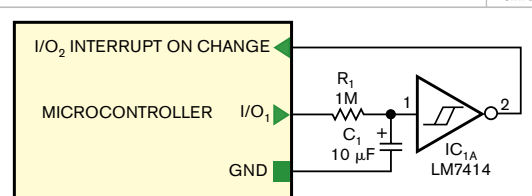


Figure 1 The RC filter along with I/O₂'s interrupt-on-change feature provides a simple and cost-effective approach for a variety of time-scale measurements from microseconds to minutes.

Sometimes, the design requires more timers without a significant cost increase. Software timers are not suitable for time-critical application because the controller is fully occupied. The circuit in this Design Idea uses the I/O "interrupt-on-change" feature that is common in most microcontrollers to implement a medium-precision, long-period timer with low additional cost.

The circuit in Figure 1 uses I/O₁, a typical I/O pin, to drive an RC filter. The circuit feeds the output of the RC filter to a Schmitt-trigger inverter whose

output goes back to I/O_2 , which has the interrupt-on-change feature. After power-up, I/O_1 is low and the output of the Schmitt-trigger inverter is high. After initialization, I/O_1 goes high. Capacitor C_1 charges up with the time constant R_1C_1 . Once it reaches logic-high voltage, the output of the Schmitt-trigger inverter goes low and triggers an interrupt on I/O_2 . In the ISR (interrupt-service routine), a counter increments, driving I/O_1 low. Now, C_1 discharges through R_1 . The voltage reaches logic low, again triggering an interrupt. As the cycle repeats, the value in the counter indicates $\text{time} = \text{counter} \times R_1C_1$. The Schmitt-trigger inverter serves as a debouncer.

Listing 1, which is available in the Web version of this Design Idea at

www.edn.com/090122dia, includes the software routine for the ATMEGA64 microcontroller from Atmel (www.atmel.com). In the **listing**, Port D, Pin 5 plays the role of I/O_1 and Pin 3, whose alternate function is INT3, plays the role of I/O_2 in **Figure 1**. The

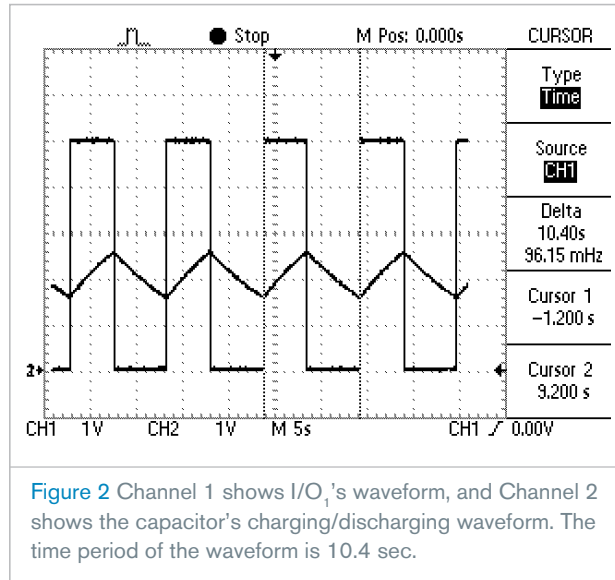


Figure 2 Channel 1 shows I/O_1 's waveform, and Channel 2 shows the capacitor's charging/discharging waveform. The time period of the waveform is 10.4 sec.

trigger-edge interrupt in this case changes from falling-rising-falling edge in a cycle. Most microcontrollers don't require this feature because any logic change will trigger an interrupt. **Figure 2** shows the timing waveform of the circuit with the ATMEGA64 and the 74HC14.

The circuit's advantages are its low cost, a microcontroller-clock-independent time period, and the ability to achieve time periods of minutes to hours by tuning resistance and capacitance. For example, with a resistance of 10 M Ω , a capacitance of 10 μF , and a 16-bit

register as a counter, you can achieve a maximum count of 75.85 days. **EDN**

ACKNOWLEDGMENT

This work is part of a system design in a project funded by the European Union under the Marie Curie Project.