

Modern ADCs improve CMOS image sensors

IC DESIGNERS HAVE IMPROVED THE ADCs INSIDE CMOS SENSORS, WHICH MUST CAPTURE FRAMES QUICKLY ENOUGH FOR HIGH-DEFINITION VIDEO. WITH THIS CONSTRAINT IN MIND, DESIGNERS MUST WEIGH THE BENEFITS OF ADC ARCHITECTURES AND MAKE TRADE-OFFS IN SPEED AND SIZE.

The last two years have seen many important developments in CMOS image sensors using a variety of architectures that employ different methods to achieve similar goals. The ADCs that the image sensors employ are keys to these architectures, with manufacturers employing one of two major approaches: pipelined or column techniques. By studying devices from Samsung (www.samsung.com), Micron (www.

micron.com), Sony (www.sony.com), Toshiba (www.toshiba.com), and STMicroelectronics (www.st.com), you can weigh the benefits of both types of ADC and decide which is best for your image-sensor application. As image sensors become more complex, they are using an increasing number of schematics in the analog paths (Figure 1). Large, stand-alone, pipelined ADCs are giving way to single-slope, integrating ADCs that align with the pixel array and contain an ADC for each col-

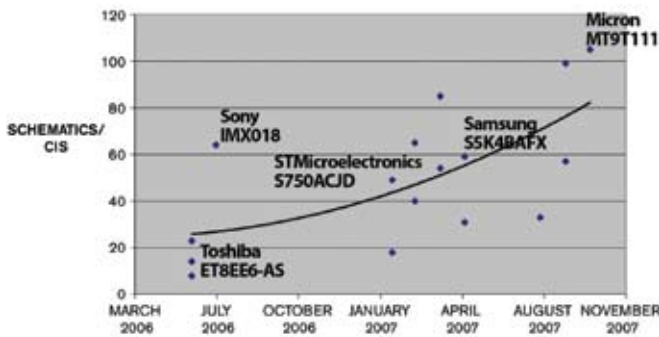
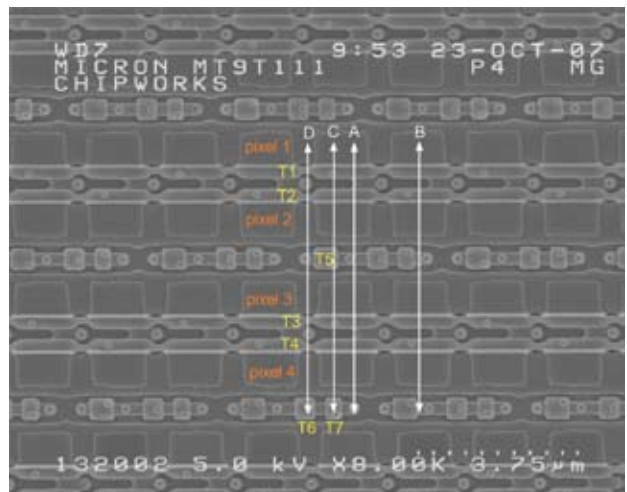


Figure 1 The number of schematics used to describe the analog paths of image sensors more than doubled in the last two years.



(a)

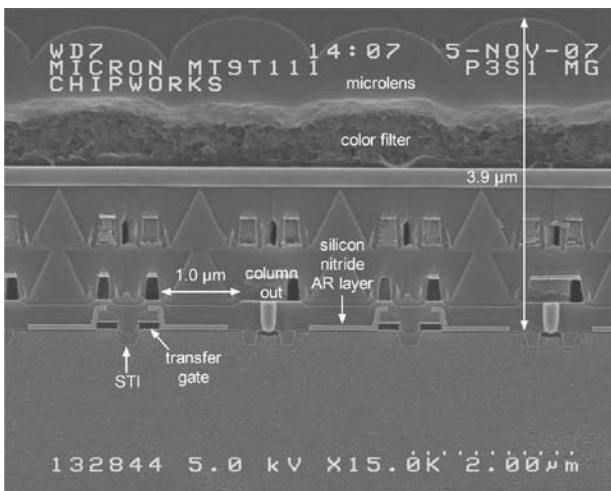
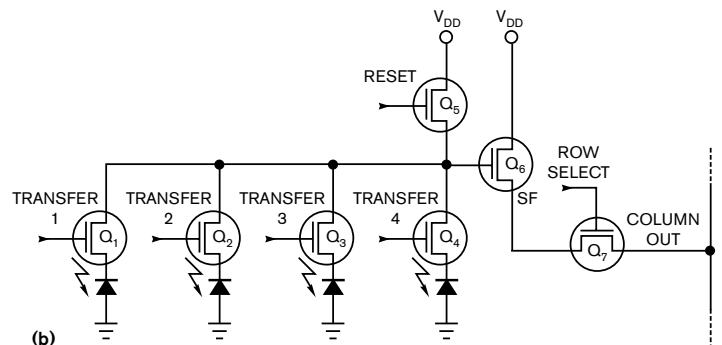


Figure 2 A SEM (scanning-electron-microscope) cross section shows the pixel array in a cell-phone image sensor.



(b)

Figure 3 An image (a) and corresponding pixel schematic (b) show the 1.75T (transistor) architecture in the Micron MT9T111 CMOS image sensor. Lines A, B, C, and D represent a cross section for subsequent analysis.

umn of the array. The benefit of this approach is that it allows you to quickly move data off the sensor. Additionally, each ADC has a much longer time to operate on a sample, thus allowing longer settling times, lower noise, and higher accuracy.

Using imaging, software-based circuitry extraction, and schematic organization, you can take apart the layers of a CMOS sensor. The newest sensors combine the pixel array, ADCs, and digital-image processing on a die. They help to move light into the pixel, often in a noisy environment, and then move that data off the array. The sensors employ microlenses to help focus the light into the “light tube,” which the readout circuitry’s metal layers partially block (Figure 2). Because today’s leading 1.4-micron pixel designs are basically twice the wavelength of visible light, this task is difficult. To reduce circuitry, manufacturers often employ transistor-sharing techniques (Figure 3).

Circuit designers try to get as many dies onto a wafer as possible. In the CMOS-image-sensor world, especially for digital-single-lens-reflex cameras, designers must take into consideration the massive die necessary for capturing a 35-mm image. In that case, designers must concentrate on improving yield rather than saving area.

PIPELINED ADCs

Developers of the first CMOS image sensors modeled the devices on CCDs (charge-coupled devices), which preceded them. These early CMOS image sensors had an architecture similar to that of CCDs. In the next stage of CMOS-image-sensor evolution, designers brought pipelined ADCs on-chip. Pipelined architecture delivered the high bandwidth necessary for processing all the pixels of the array. Although these ADCs have long latencies, these delays are not problematic in this application. Early on-chip ADCs used a single simple pipelined design (Figure 4). These ADCs gradually evolved to the current state-of-the-art DDR (double-data-rate), fully differential, multiple-pipelined ADCs. The analog-signal path from the light-collecting photodiode to the ADC is now fairly standard across the industry. The chip electronics must select a single

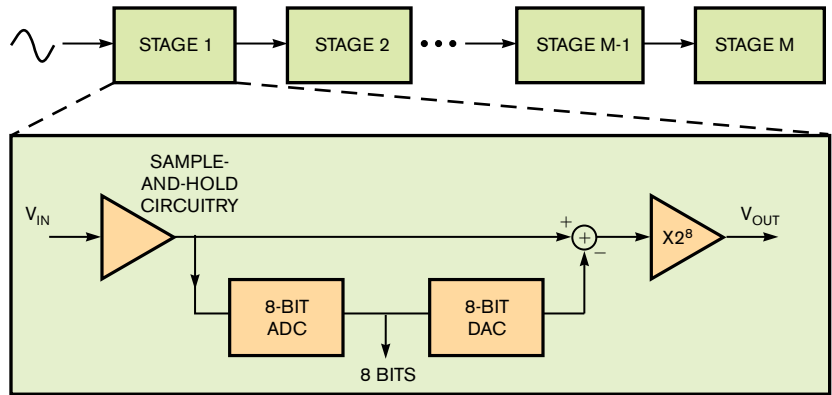


Figure 4 A pipelined-ADC architecture consists of repeated stages.

row of pixels, transfer the signals to column circuits, perform correlated double sampling, and then sample and hold the resultant signals.

Many manufacturers now use this architecture to reduce the number of transistors in the array. The Micron MT9T111 1.75T, for example, employs seven transistors and four photodiodes (Figure 3). When system electronics activate the row-select signal, the chip connects the selected row of pixels to the column-out line. These signals travel to the edge of the array in

which the pitch-matched column-parallel-sampling circuits reside. The signal typically first reaches a multiplexer, allowing multiple columns of pixels to use the same analog-processing column. This approach also allows the selection of only a subset of pixels during high-speed image capture for preview and downscaling, or “binning.” Active loads are also present at this point to bias and clamp the signals.

The image signals then enter the correlated-double-sampling circuit (Figure 5). Metal layers shade some photodi-

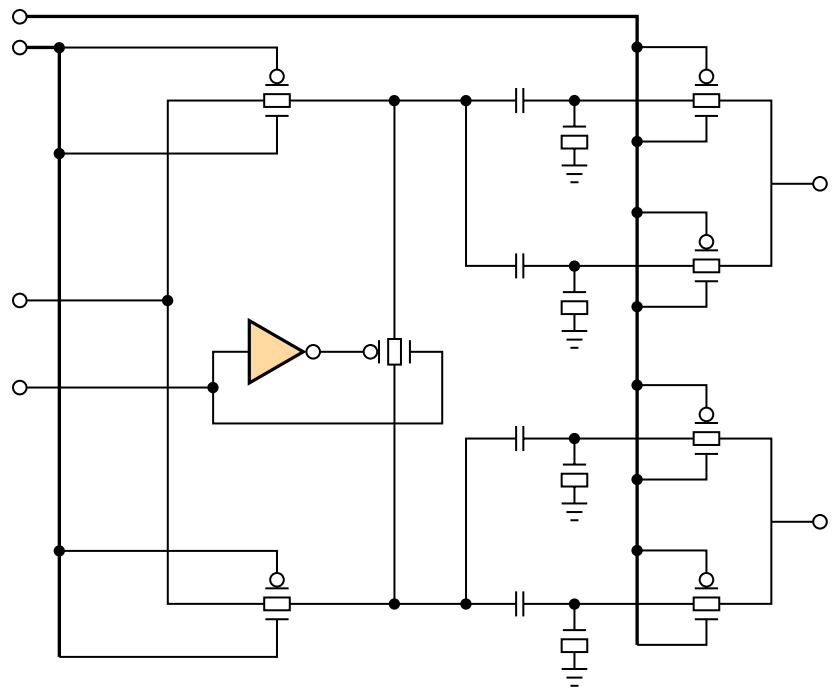


Figure 5 The Micron MT9E001 uses a modern correlated-double-sampler design.

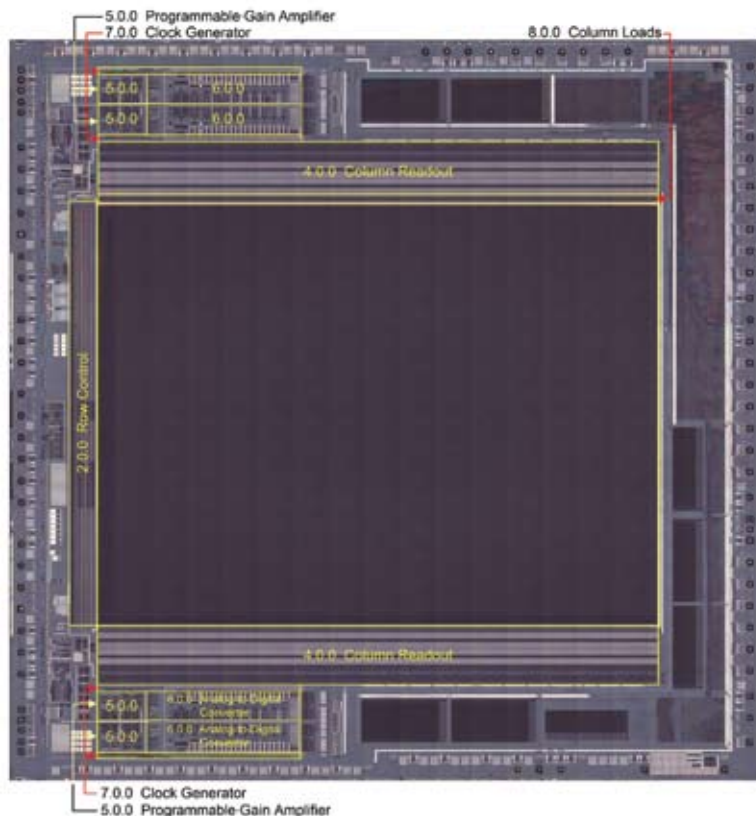


Figure 6 The Micron MT9E001 uses four pipelined ADCs.

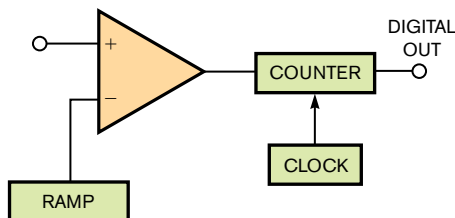


Figure 7 The single-slope integrating-column ADC finds use in most CMOS image sensors.

odes, which the circuitry reads to establish the black levels along the row. Next, the circuitry samples the actual data signal and subtracts the black level to give the output level. At this point, the pipelined ADC architecture multiplexes the signals from the pitch-matched column circuits to the ADCs. As speed and bandwidth requirements have increased, IC designers have added more ADCs. For example, the Micron MT9E001 for digital cameras uses four 12-bit ADCs (Figure 6).

Both the MT9E001 and the MT9T111 use a DDR, fully differential-pipelined scheme. The parts can achieve a 96-Mbps data rate at 400-mW power consumption. One feature of the DDR scheme is that dual-pipelined ADCs share the operational amplifier, allowing the chip to acquire two samples and perform two conversions in one clock cycle. No dc-bias current goes unused during the sampling phase of the operation. A key disadvantage of this architecture is layout difficulty (Reference 1). However, capacitor matching in this device is adequate for achieving 12 bits of accuracy without digital correction (Reference 2). The four DDR, 12-bit pipelined ADCs on the chip make it possible for the MT9E001 to exceed the speed of CCDs.

COLUMN ADCs

Consumers found that early digital cameras had unacceptably long lag

times, making it difficult to quickly take a series of consecutive pictures. To address that problem, manufacturers developed column-parallel ADCs, which allow the CMOS sensor to take pictures at 60 frames/sec in the pitch-matched column area. For example, the 2M-pixel Samsung S5K4BAFX CMOS image sensor for cell-phone cameras has 882 parallel ADCs. In this design, the ADCs are small and the speed-per-ADC requirement is low. Column-parallel ADCs use single-slope integrating-ADC architectures (Figure 7). Only the comparator and the counter need to be in the column pitch. The devices can generate the ramp-reference signals and clocks outside the column, and all the ADCs can share these signals and clocks. As in the pipelined-ADC architecture, column ADCs multiplex the signal and then apply active loads. The usual correlated double sampling then takes place.

At this point in the signal path, the designs diverge. In the column-parallel-ADC architecture, the pixel signal goes to one input of a comparator, in which the other input is a ramp voltage. The output of this comparator acts as the enable signal to a counter. This counter synchronizes with a master counter to create the ramp signal. When the ramp voltage exceeds the pixel voltage, the comparator flips, and the counter becomes disabled. The counter then holds the digital value corresponding to the

analog pixel voltage on 882 columns in parallel.

This architecture allows for small and simple ADCs in the column pitch and moves the accuracy and speed constraints to the ramp generator. This ramp generator must now accurately and quickly convert a digital value that a counter creates to an analog voltage to act as the ramp. Because the S5K4BAFX has a 10-bit ADC, the ramp-generator DAC must accomplish 1024 conversions for the 882 ADCs to convert their value at a faster rate than one ADC could operate. To accomplish this task, the first 10-bit column-parallel ADCs employed flash DACs using resistor dividers as the ramp generator. The Samsung S5K4BAFX has a subranging resistor divider, a coarse voltage divider of 16 resistors, a fine voltage divider of 16 resistors, and an LSB-resistor string of four resistors, resulting in the required 1024 levels (Figure 8).

NEXT-GENERATION ADCs

Samsung was the first manufacturer to introduce an advanced column ADC. In 2007, the company released the S5K4C1GX 3Mp CMOS image sensor, employing a 12-bit ADC, for mobile phones. Samsung manufactured the device in a 90-nm process, and it uses a similar single-slope integrating-column ADC as in the previous generation, including a comparator and a 13-bit counter. The 13 bits allow for a full

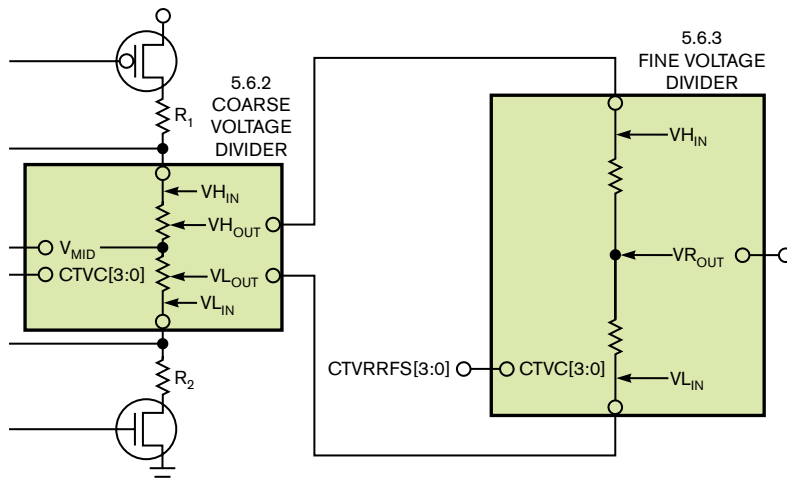


Figure 8 The Samsung S5K4BAFX resistor-divider ramp generator can generate 1024 levels.

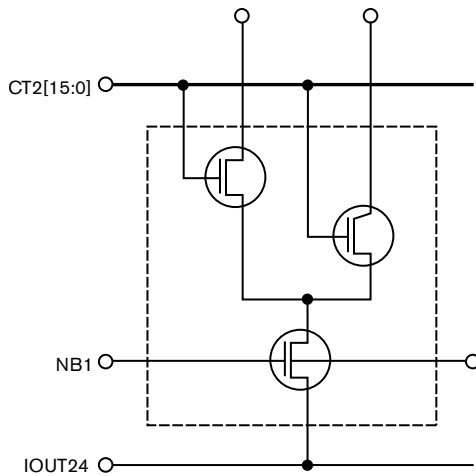


Figure 9 The Samsung S5K4C1GX current-steering DAC cell replaces previous resistor-string designs.

12-bit value plus overflow. The part's ramp generator uses a current-steering DAC to replace the resistor-string DAC of the previous generation (**Figure 9**). This innovation is significant because current-steering DACs are more complex and occupy more area. For a 12-bit ADC, the need for precision in the reference voltage is great enough to require the complexity and additional space of the current-steering DAC. Samsung uses three current-steering arrays and combines their outputs in a fourth array. Each array is a stand-alone current-steering DAC, including an array of unity-current sources and their respective steering transistors. A fully decoded 13-bit counter drives the array.

Sony in 2007 announced its first CMOS image sensor employing a column ADC; the company's previous sensors employed pipelined ADCs. Today, three Sony CMOS image sensors—one for mobile phones, one for digital-single-lens-reflex cameras, and one for camcorders—use column ADCs. Surprisingly, the design is not specific to high-frame-rate applications. Sony has taken this architecture one step further in the IMX017 camcorder CMOS-image sensor. The device uses a digital, rather than

analog, correlated-double sampling circuit. Rather than storing the black pixel voltages on a capacitor for later subtraction from the signal, the device samples the black pixels directly on the ADC comparator. The device then compares these black signals with the ramp voltage, and the counter counts down during this phase until the ramp voltage crosses the black signal and the counter stops. The unit then applies the pixel voltage to the comparator, and the counter starts counting up, effectively subtracting the black signal from the pixel value. This

digital architecture eliminates the need for large sampling capacitors and reduces switching noise.

CMOS-image-sensor commercialization has been rapid. One or two players do not dominate the market. The result is a range of innovation, as the small but important ADC demonstrates. Expect market convergence within the next three to five years. Meanwhile, tracking the major designs will be interesting.**EDN**

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