

# designideas

READERS SOLVE DESIGN PROBLEMS

## Convert signals to proper logic levels

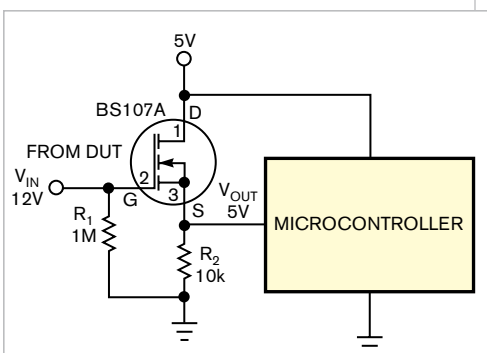
Abel Raynus, Armatron International Inc, Malden, MA

When designing a test station incorporating a microcontroller, you often face voltages in the test that exceed the maximum input level permitted for the microcontroller. For example, if a microcontroller uses a 5V power supply, then the maximum input signal should also be 5V. When a test voltage exceeds 5V, you might think to reduce the voltage with a voltage divider. A voltage divider can influence the DUT (device under test), however. So, a signal conditioner needs high input impedance. Also, the signal conditioner's output signals should match the logic levels of the microcontroller despite some fluctuation of the measured signal. It allows you to use the regular microcontroller-input pins instead of ADC ones.

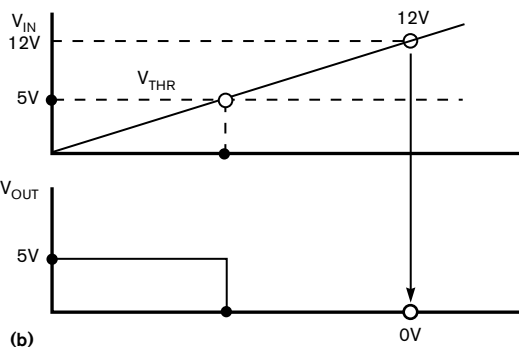
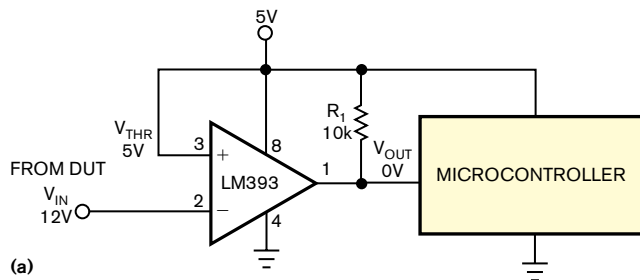
Engineers often use a noninverting op amp to bring signal voltages in line. However, most op amps have differential-input-voltage ranges matching their power-supply voltages. Thus, you need one more power-supply voltage with a higher voltage and several extra resistors to lower the op amp's

output to the microcontroller level. Moreover, the output will follow the measured input-signal variations, so it needs analog-to-digital conversion in the microcontroller.

A better approach is to use a small-signal MOSFET in the voltage-repeater configuration (**Figure 1**). You can use the BS107A from On Semiconductor ([www.onsemi.com](http://www.onsemi.com)) for this task. You can consider the gate-to-source area of the MOSFET as a capacitor with a value of approximately 60 pF. To discharge it in the absence of the DUT, connect a resistor of ap-



**Figure 1** You can use a small-signal MOSFET to provide overvoltage-signal conditioning.



**Figure 2** Another approach to signal conditioning is to use dual- or quad-voltage comparators (a). The 5V power-supply voltage acts as the positive-threshold voltage. The output is 5V for input signals lower than this level. If the input signal exceeds 5V, the output voltage drops to 0V (b).

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proximately  $1\text{ M}\Omega$  between the gate and ground. Also, the input voltage should be more than the MOSFET's gate-threshold voltage,  $V_{\text{THR}}$ , of 3V dc but less than the maximum rated gate-to-source voltage,  $V_{\text{GS}}$ , of 20V dc. In this figure, the output voltage never exceeds the power-supply voltage, and variations of the input voltage have no effect on output as long as they happen in the saturation region. A drawback of this approach is that you must use as many transistors as the number of test-points in the DUT.

Another good option is to use any dual- or quad-voltage comparator. You can use an LM393 from National Semiconductor ([www.national.com](http://www.national.com)) because it's inexpensive and widely available. Figure 2 shows a simple configuration with few components. The 5V power-supply voltage acts as the positive-threshold voltage. The output is 5V for input signals lower than this level. If the input signal exceeds 5V, the output voltage drops to 0V. Resistor  $R_1$  connects an open collector of the LM393 to the supply voltage.

Sometimes, a zero-output signal is undesirable. A missing power-supply voltage, a bad solder joint, or a broken wire in the test fixture could cause this zero-output signal. Use a logic high level when the signal under test is present and logic low when it's absent. At first glance, it seems that just

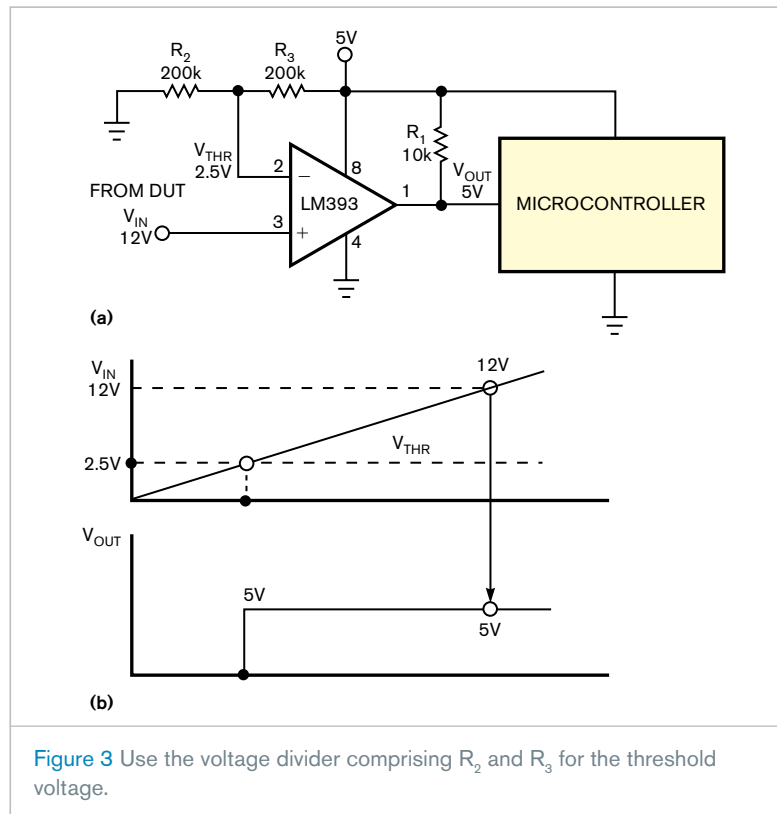


Figure 3 Use the voltage divider comprising  $R_2$  and  $R_3$  for the threshold voltage.

switching the comparator pins of the input and the threshold voltages provides an acceptable approach. However, that assumption is invalid because the positive input voltage may exceed the power-supply level only as long as the other voltage remains within the

common-mode range. The upper limit of common-mode input voltage for the LM393 is 1.5V less than the power-supply voltage, or 3.5V. Thus, you should use the voltage divider comprising  $R_2$  and  $R_3$  for the threshold voltage (Figure 3).EDN

## DDR-differential-clock source on SOC drives two DDR-memory chips

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Many system engineers assume that a differential-clock source should drive just one chip. If a system design requires driving two DDR-memory chips, however, the design would inevitably need a differential-clock buffer. This Design Idea describes a circuit that drives two DDR chips without a clock-source buffer yet does not sacrifice much of the signal integrity.

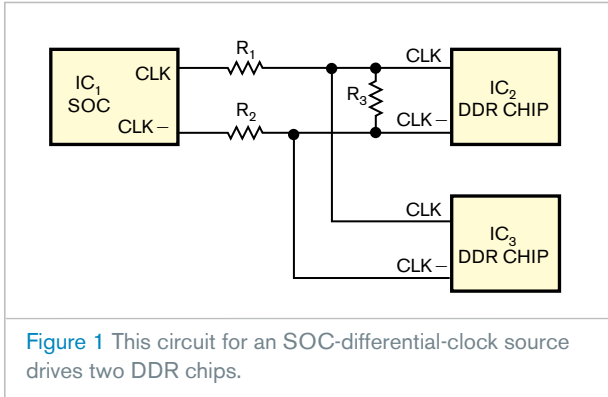
The cost-saving nature of an SOC

(system-on-chip) design dictates the need for fewer pins. Such designs typically have only one pair of differential signals available for external-memory-chip connection. When the system design requires more than one DDR chip, designers typically use a clock buffer.

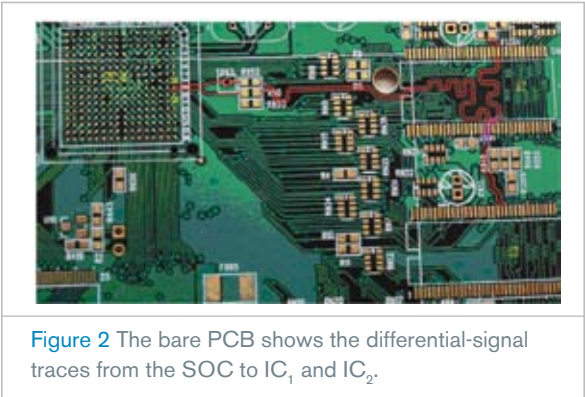
Figure 1 shows an SOC with an embedded DDR controller, which connects the SOC's differential clock to two DDR-memory chips. Differential

signals CLK and CLK- from SOC chip  $IC_1$  connect to series resistors  $R_1$  and  $R_2$ , respectively. The differential traces then connect to DDR-memory chips  $IC_2$  and  $IC_3$  with a  $120\Omega$  termination resistor near  $IC_2$ .

Figure 2 shows the equivalent PCB (printed-circuit-board) layout. The PCB comprises a four-layer FR4 material with a ground plane under differential lines CLK and CLK-. The CLK and CLK- signals are routed close to each other and pass through series resistors  $R_1$  and  $R_2$ , which are also placed close to each other, to provide proper termination. The closely spaced differential signals connect to



**Figure 1** This circuit for an SOC-differential-clock source drives two DDR chips.



**Figure 2** The bare PCB shows the differential-signal traces from the SOC to IC<sub>1</sub> and IC<sub>2</sub>.

IC<sub>2</sub> with the 120Ω termination resistor, R<sub>3</sub>. The bottom-layer traces are necessary to connect the differential signals to IC<sub>3</sub>. The total length of the differential pair is approximately 2.5

in. from the SOC chip to the DDR chips.

The SOC provides DDR differential clocking. With various values for R<sub>1</sub>, R<sub>2</sub>, and R<sub>3</sub>, the best results occur when R<sub>1</sub>

and R<sub>2</sub> are 0Ω and R<sub>3</sub> is unconnected. Figures 3 through 7, which are available with the Web version of this Design Idea at [www.edn.com/090205dia](http://www.edn.com/090205dia), show various waveforms for the signals. **EDN**

## Flying capacitor and negative time constant make digitally programmable-gain instrumentation amplifier

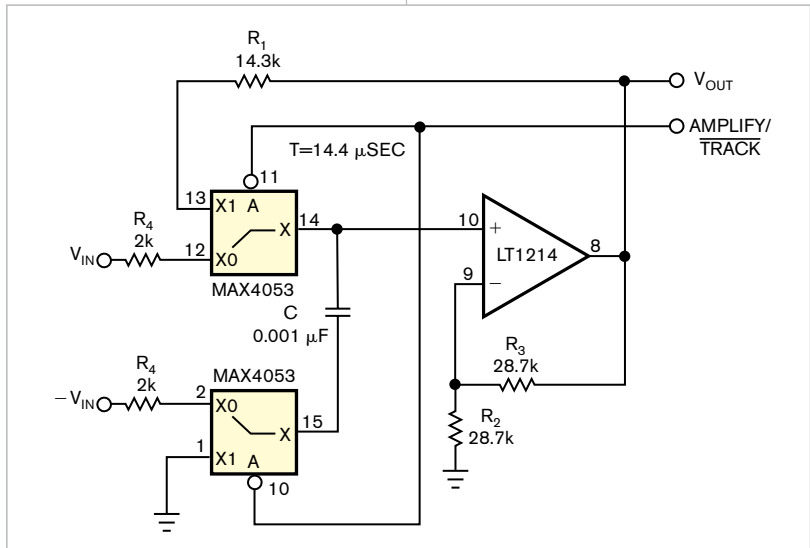
W Stephen Woodward, Chapel Hill, NC

Numerous and evil are the forces of darkness that conspire to frustrate accurate analog-to-digital conversion of wide-dynamic-range analog signals. Among these gremlins lurk common-mode-voltage noise and signal amplitudes too variable to fully use ADC-input span and conversion resolution. Proven charms against common-mode noise are differential inputs, and you can exercise variable signal amplitudes by implementing digitally programmable gain. DPGIAs (digitally programmable-gain instrumentation amplifiers) combine both useful features (**Figure 1**).

Microcircuit—even monolithic—DPGIAs, such as the Linear Technology ([www.linear.com](http://www.linear.com)) LTC6915, are available. But this Design Idea describes a DDENT (differential-divergent-exponential-negative-time-constant) DPGA employing the concepts of the “flying”-capacitor differential input and the DDENT curve, which provide an interesting alternative.

You control DDENT operation with the amplify/track-bit mode. Track mode connects flying-capacitor

C to the positive and negative differential-input terminals, which acquire the input voltage, V<sub>IN</sub>. The transition to the amplify mode isolates C from the input and initiates regenerative negative-time-constant exponential amplification of the input voltage. From that point (**Reference 1**) until the moment when a connected ADC ultimately samples and converts the



**Figure 1** The behavior of the RC topology is still simple when you replace the resistors with an active circuit that synthesizes a negative resistance.

output voltage,  $V_{OUT}/V_{IN}$  is a divergent exponential function of time:  $gain = 2^{(t/10 \mu\text{sec} + 1)}$ .

Building on the assets of that earlier design, this new circuit features CMR (common-mode rejection) that neither resistor-network matching nor the CMR of the op amp limits. Stray-capacitance issues impose the only limits, but you can minimize these issues with careful circuit layout. The circuit has rail-to-rail inputs, virtually unlimited programmable gain, and gain-set resolution that only the resolution of the amplify-interval timing limits. The circuit also has settling time 10 to 100 times faster than that of the

## THIS NEW CIRCUIT FEATURES CMR THAT NEITHER RESISTOR-NETWORK MATCHING NOR THE CMR OF THE OP AMP LIMITS.

exemplary LTC6915 and  $\pm 10\text{V}$  output-amplitude capability—two to four times greater than that of monolithic DPGIAs. Besides the inherent dc ac-

curacy of the op amp you choose, the accuracy and repeatability of the timing of exponential generation, ADC sampling, and RC-time-constant stability are the only limits on the amplifier's signal-processing performance and precision. In the sample circuit, in which  $T = 14.4 \mu\text{sec}$ , 1 nsec of amplify-timing error or jitter equates to 0.007% of gain-programming error. **EDN**

### REFERENCE

1 Woodward, W Stephen, "Digitally programmable-gain amplifier uses divergent-exponential curve," *EDN*, Jan 8, 2009, pg 49, [www.edn.com/article/CA6625454](http://www.edn.com/article/CA6625454).

## MOSFET prevents battery damage

Santosh Bhandarkar, Wep Peripherals, Mysore, India

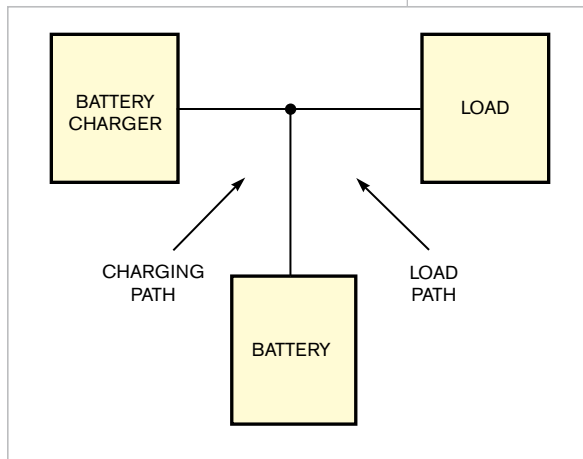
Sealed-lead-acid batteries, which find wide use in power-electronics products, such as UPS (uninterruptible-power supplies), inverters, and emergency lamps, supply power to the load whenever utility power is unavailable. When you restore utility power, a charger supplies the power to the load and charges the batteries (**Figure 1**).

You can add a diode to protect a load from current resulting from a reverse-

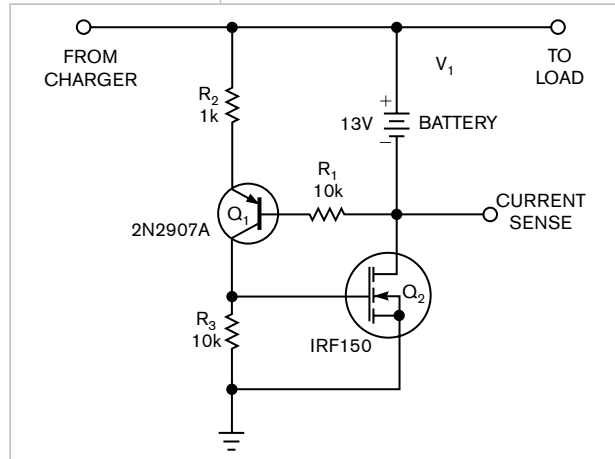
connected battery. The diode, however, won't protect a reverse-connected battery from the charger circuit. If the charger is on, a potentially dangerous current can flow into a reverse-connected battery. The battery voltage, which normally opposes the charging voltage, now aids it, which lets a higher current flow into the battery.

If you add an N-channel MOSFET to the circuit, you can protect the battery from this damaging condition

(**Figure 2**). The MOSFET conducts only when the battery is correctly connected, which lets the battery charge or discharge. In this condition, the transistor gets forward-biased, which switches on the MOSFET. If the battery is reverse-connected, the transistor and MOSFET turn off, thus preventing current flow. This simple circuit provides reverse-battery protection in both charger and battery paths, thereby protecting the battery, the charger, and the load. You can use a microcontroller to measure battery current and make a decision on appropriate action, as well. **EDN**



**Figure 1** Batteries provide power to a load when utility power is off.



**Figure 2** MOSFET  $Q_2$  protects the battery from excessive current.

# Voltage doubler improves accuracy

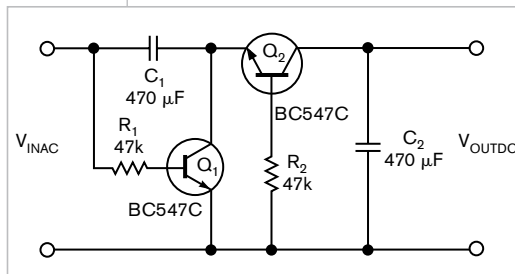
S Chekcheyev, Tiraspol, Moldova

The voltage doubler in **Figure 1** provides more accurate voltage doubling than does the conventional voltage doubler in **Figure 2** because it uses transistors instead of diodes. You can express the output voltage of the conventional doubler as  $V_{OUTDC} = 2V_{INAC} - 2V_D$ , where  $V_{OUTDC}$  is the output dc voltage,  $V_{INAC}$  is the amplitude of the input ac voltage, and  $V_D$  is the voltage across the forward-biased diodes. The error of the conventional voltage doubler is  $2V_D$ . Transistors  $Q_1$  and  $Q_2$  in **Figure 1** are saturated during the positive and the negative half-cycles, respectively, of the input ac voltage. The operation of the saturated transistors is similar to the operation

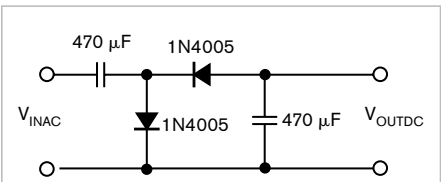
of the forward-biased diodes in **Figure 2**. The collector-emitter voltage of the saturated bipolar transistors, however, is substantially smaller than the voltage across the forward-biased diodes. Thus, the error of doubling decreases.

Transistors  $Q_1$  and  $Q_2$  are reverse-biased during the negative and the positive half-cycles, respectively. The re-

verse beta of the bipolar transistors is small; consequently, the operation of the reversed transistors in **Figure 1** is similar to the operation of the reverse-biased diodes in **Figure 2**. Both circuits underwent tests with a resistive load of  $10\text{ k}\Omega$  and a 50-Hz, 2V-amplitude sinusoidal signal applied to the input. The measured output voltage of the conventional voltage doubler was 2.8V, and the error of doubling was  $2 \times 2\text{V} - 2.8\text{V} = 1.2\text{V}$ . The measured output voltage of the proposed voltage doubler was 3.8V, and the error of doubling was  $2 \times 2\text{V} - 3.8\text{V} = 0.2\text{V}$ . **EDN**



**Figure 1** An improved voltage doubler uses transistors for better accuracy.



**Figure 2** A conventional voltage doubler uses diodes.