



BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

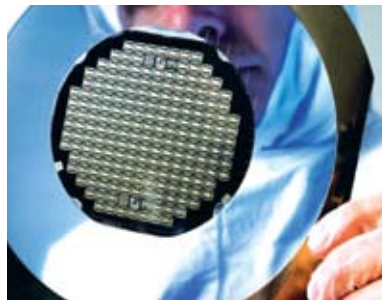
Mitigating tapeout risk

The last few process-technology nodes emerged after major shifts in technical and physical complexity and rising manufacturing costs. During these shifts, chip-design teams have had the constant availability of expert personnel, design tools, and computing/IT resources that were sufficient to complete the projects. Recent economic conditions, however, have eroded the availability of these infrastructure resources.

Most physical-design engineers focus on the performance aspects of the design rather than the whole flow. Downsizing or divisional restructuring, however, quickly disrupts the sign-off loop for a design release. Most companies have a manual sign-off-review process during which experts from design engineering, physical design, and manufacturing/operations review the physical design and design verification and determine whether the product is ready for release. Some of these personnel are familiar with the project. Companies must capture the knowledge of these key people and incorporate it into an automated sign-off-release procedure.

One of the biggest issues is the availability of a manufacturing-knowledgeable staff to participate in this review. The in-house-wafer-fab business model has in-house expertise for this manufacturing interface. Most companies have lost this resource, however, because they use wafer foundries as their suppliers. To minimize risk, companies should now include the foundries' technical representatives in the results-review portion of the release procedure. Including these people avoids the need for multiple sign-off cycles after the receipt of the design data and before the start of manufacturing. The

Companies should now include the foundries' technical representatives in the results-review portion of the release procedure.



companies should make these foundries partners in the flow rather than hold them at a distance as they would subcontractors or suppliers.

Restructuring at many semiconductor-design groups has resulted in a large reliance on reuse of known-good blocks in new designs. When the designer originally responsible for the blocks is available, this method is known and proven and reduces risk. Loss of the oversight of the original

designers orphans a great deal of the data for these blocks, leaving design data without context. Without that context, reusing this data in another application is risky. Doing design-application checking and statistical sensitivity analysis in the physical-verification portion of the design can reduce this risk. Several new software tools from such companies as Mentor Graphics (www.mentor.com) and Solido Design Automation (www.solido.design.com) address this market.

Current process technology at the 65-, 45-, and 40-nm nodes has a high cost of manufacturing and requires large design teams to effectively use the many available devices. Most applications do not require huge numbers of devices, however. Also, many function blocks—standard interfaces such as SATA (serial advanced technology attachment), 802.11, USB (universal serial bus), and HDMI (high-definition multimedia interface)—also have known, tested, and validated intellectual property in older process technologies, such as 250, 180, 150, 130, and 90 nm. So, you can both offset a great deal of risk and save money by targeting these older process-technology nodes. These older nodes also have the advantage of well-defined flows and stable software tools.

One easy-to-implement factor for reducing risk on a new tapeout is to increase the number of available power and ground pairs. Designs with lower power-supply voltages and multiple power modes have lower PSRRs (power-supply-rejection ratios) and higher noise floors. Adding power and ground pairs and creating power and ground islands help minimize and isolate the noise. An added benefit is that you can more finely tailor testing and debugging as the increased power resources minimize interdependencies among the blocks. **EDN**

Contact me at pallabc@siliconmap.net.

www.edn.com/tapeout