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Buck converter uses low-side PWM IC

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The most common switching-power topology is a buck converter, which efficiently transforms high voltages to low voltages. **Figure 1** shows a typical buck converter in which the N-channel MOSFET, Q_1, needs a floating-gate drive signal. The floating-gate drive is part of the PWM (pulse-width-modulation) controller IC. Q_1 can be either N or P channel, depending on the controller's design. Unfortunately, the IC's voltage rating must be as high as the input voltage, which places a limit on the maximum voltage it can process.

The circuit in **Figure 2** uses a simple voltage-level shifter that lets a buck converter control a pass transistor with a low-side IC that has a ground-referenced gate drive. Because the level-shifting circuit in the PWM IC does not have to tolerate high voltages, you can implement a converter with an arbitrarily high input voltage.

PWM ICs with low-side gate drivers can power N-channel MOSFETs that are on when they have a positive gate-to-source voltage. The circuit in **Figure 2** uses a P-channel device as the high-side MOSFET; it's on when its gate-to-source voltage is negative. Therefore, you must invert the control signal from the PWM controller. A MOSFET totem-pole configuration comprising Q_2 and Q_3 will work, although you can also use an inverting-gate driver.

Capacitor C_2 performs the level-shifting. It must have a value large enough to maintain its charge at the switching frequency but small enough for its voltage to follow variations in the input voltage. Resistor R_1 and P-channel MOSFET Q_3 charge C_2 to a voltage of $V_C = V_{IN} - V_{CC}$, where V_C is C_2's voltage, V_{IN} is the input voltage, and V_{CC} is the supply voltage of the Q_2 and Q_3 totem-pole configuration and the PWM IC. The supply voltage must be less than zener diode D_2's breakdown voltage. Otherwise, current will flow through D_2 and C_2 whenever Q_2 is on, which lowers efficiency. D_2 limits C_2's voltage to the value in the above **equation**. When Q_3 is on, D_2 becomes forward-biased if the voltage attempts to increase. This circuit applies a 0V voltage between Q_1's gate and source when Q_3 is on, and it applies $-V_{CC}$ when Q_2 is on.

Resistor R_1 also ensures that Q_1's gate-to-source capacitance discharges, which keeps Q_1 off when the totem pole's output

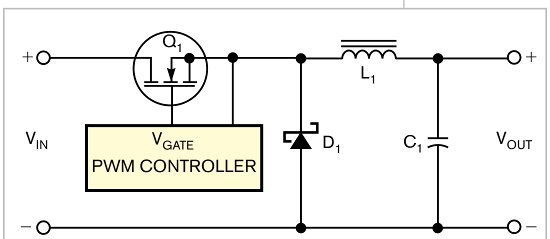

Figure 1 A basic buck converter uses a PWM controller and a MOSFET.

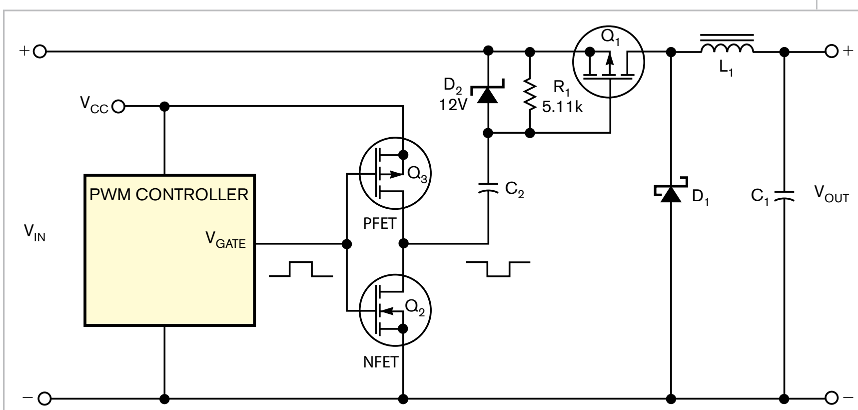

Figure 2 A level-shifting circuit provides low-side control of a buck converter's high-side FET.

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voltage is high. Diode D_2 limits Q_1's gate-to-source voltage to 12V regardless of the circuit's input voltage. Capacitor C_2 is transparent to Q_1's gate-drive pulse, so the circuit's gate-driving capability is just as good as that of the totem-pole circuit itself. The level shifting, therefore, imposes no limitation on the size of the MOSFET that the circuit can drive.

Figure 3 shows a practical buck converter employing this scheme. The converter's input voltage is 18 to 45V, and its output voltage is 12V at a 1.5A output current. The converter uses National Semiconductor's (www.national.com) LM5020-1 flyback/boost/forward/SEPIC (single-ended-primary-inductance-converter) PWM-controller IC.

The **figure** retains the component designators from the previous **figures** but adds functions such as input-voltage filtering in C_9; input-undervoltage lockout in R_2 and R_7; soft-start capability in C_3; switching-frequency-setting ability in 12.7-kΩ R_3 for 500 kHz; feedback compensation in C_7, C_8, and R_6; and output-voltage setting in R_9 and R_{10}.

The LM5020-1 provides current-mode control, but, in this circuit, it implements voltage-mode control. An internal sawtooth-current source with a peak value of 50 μA, which adds slope compensation to a current signal, serves as a voltage ramp. This current flows through 5.11-kΩ resistor R_4 and an internal 2-kΩ resistor to generate a ramp with a peak-to-peak voltage of 50 μA×(2 kΩ+5.11 kΩ)≃300 mV at the CS pin, Pin 8. The COMP pin, Pin 3, compares this sawtooth to the output error voltage at the COMP pin, which generates the right duty-ratio signal for Q_1.

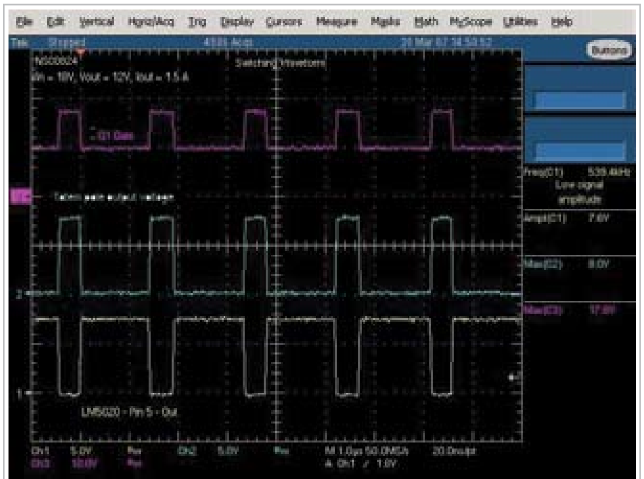

Figure 4 Voltage waveforms in the buck-converter circuit of Figure 3 show clean voltages with short rise and fall times.

Figure 4 shows the circuit's switching waveforms. Oscilloscope channel 1 (bottom trace) shows the gate-drive signal that the LM5020-1 generates. Channel 2 (middle trace) shows the corresponding totem-pole output voltage. Channel 3 (top trace) shows the level-shifted totem-pole output voltage between the source and the gate of Q_1. The peak value of Q_1's gate-to-source voltage equals the input voltage, and its amplitude is about 8V, the value of the supply signal that the LM5020-1 internally generates. All the waveforms are clean and have short rise and fall times. The full-load efficiency of the circuit is 86 and 83% at input voltages of 18 and 45V, respectively.EDN

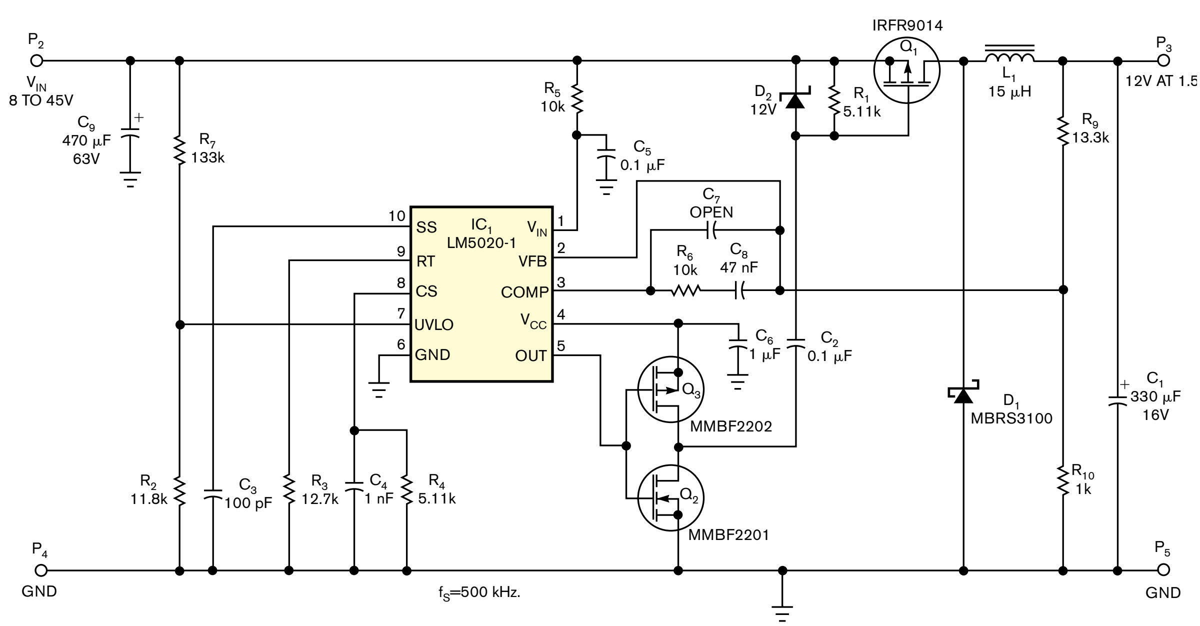

Figure 3 An alternative buck converter uses a low-side PWM IC to control MOSFET Q_1.

Isolated clock source acts as test generator

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Circuits such as PLL synthesizers, high-dynamic-range ADCs, and timing-sensitive digital networks require stable and spurious-free clocks. Testing these circuits is a difficult task when you use a master oscillator, even if the signal theoretically matches the application's phase noise and spurious responses. Variable clock-line loads, typical conditions in circuits under functional evaluation, and power-supply-line interferences, again typical in open-board environments on lab desktops, can degrade signal purity with jitter or unpredictable phase steps.

You can insulate an oscillator from a load requiring a special high reverse-attenuation-buffer stage, but it is more difficult to implement this insulation at frequencies of 10 MHz and more. This Design Idea describes a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

The circuit uses a quartz-oscillator stage with two NPN transistors in a conventional scheme (**Figure 1**). You select components C_3 and C_4 relative to the frequency; for 15- to 30-MHz frequencies, the corresponding values are 220 and 100 pF, respectively. You can scale up these values for lower frequencies. You can also substitute this stage with other equivalent circuits. A level-shift follower uses PNP transistor Q_3; a TTL-compatible signal at the output is available. You select resistor R_7 for the best pulse response; a value of 22Ω is adequate for most applications; however, you can omit the resistor if necessary.

You now apply a logic-level signal to the input pin of a high-speed CMOS optocoupler, IC_2. This design uses an HCLP-7101 type that operates at frequencies as high as 40 MHz, but new devices, such as the HCPL-77xx in SMD packages, are fully compatible. These optocouplers have input-to-output capacitance of less than 1 pF, and they have separate supply pins. If you do not use common grounds, as in the **figure**, you establish an optimized ultralow-power coupling, which provides effective isolation from load conditions and EMI (electromagnetic interference) that otherwise might modulate the incoming signal.

Note that the left side of the circuit, comprising an oscillator and the input half of the optocoupler, uses a dedicated battery to obtain the 5V supply voltage. On the right side, comprising the output half of the optocoupler, all lines directly connect to the board under test with relatively long cables; thus, they cause no disadvantages in the oscillator stage. You can use any optocoupler of adequate bandwidth as long as you pay attention to the correct power-supply voltage and the logic-level compatibility of IC_2. EDN

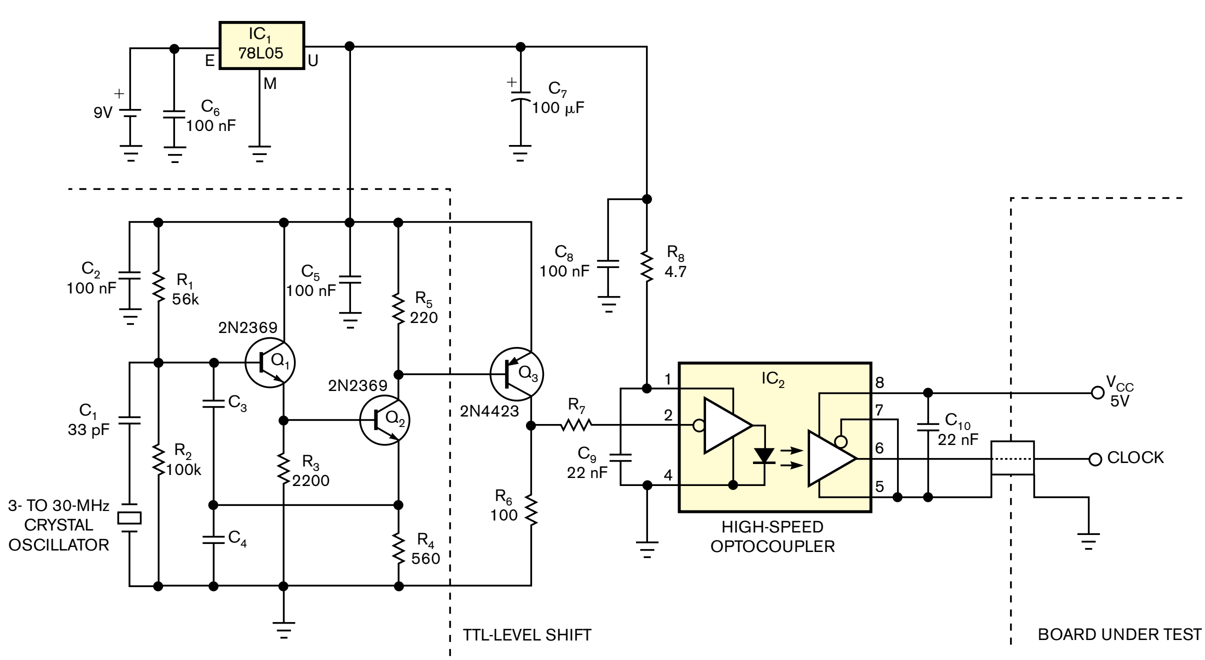

Figure 1 This circuit provides a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

Class AB inverting amp uses two floating-amplifier cells

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Transistors often find use as three-pin amplifier devices, in which the input and the output share one pin. Thus, the input and the output must have the same voltage at this pin. On the other hand, a four-pin amplifier could isolate the circuit's input and output. Using optoisolators, you can design a four-pin Class AB amplifier. Although the output voltage of an optoisolator curtails its usefulness, you can add discrete transistors to form an isolated amplifier.

Figure 1 shows an example of a simple, 1-kV-p-p Class AB inverting amplifier that uses two identical floating-amplifier cells. The frequency response is dc to 20 kHz at full gain. You can achieve higher frequencies but at lower gains. The ratio of resistors R_2 and R_1 sets the gain. This circuit eliminates the need for many voltage-shifting components, which are typical of a standard circuit design. The positive and the negative cells are driven out of phase. The 15V and −15V and re-

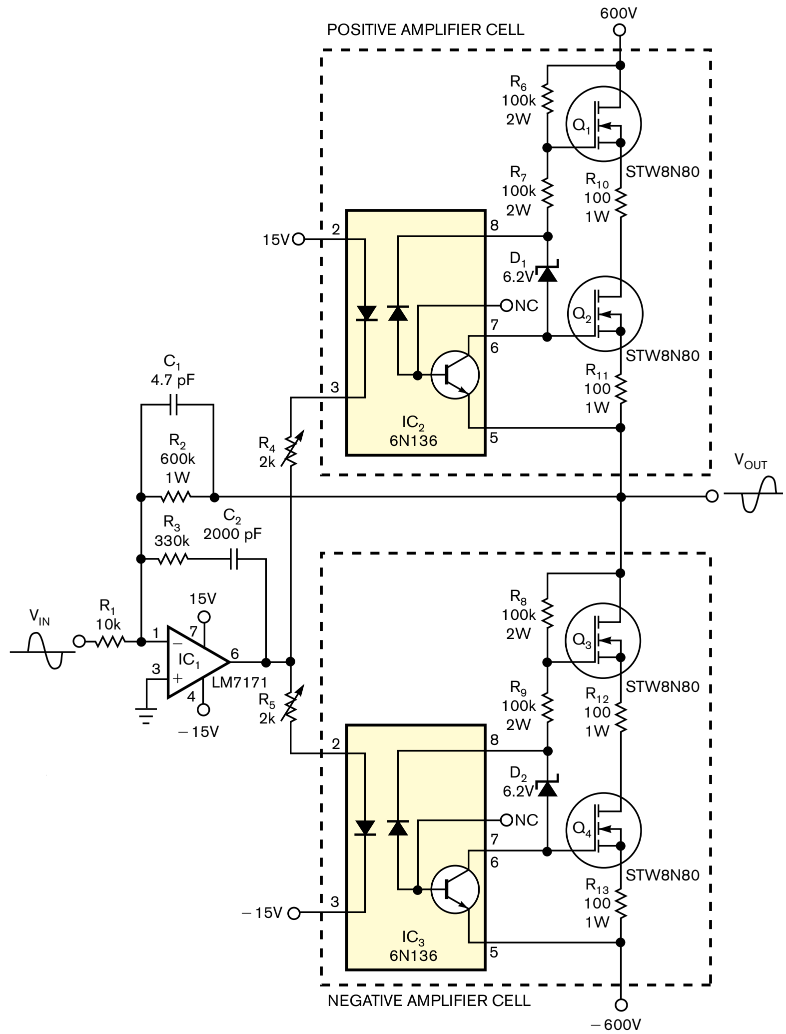

Figure 1 Transistors boost the output voltage and current of optoisolators, making an isolated amplifier output.

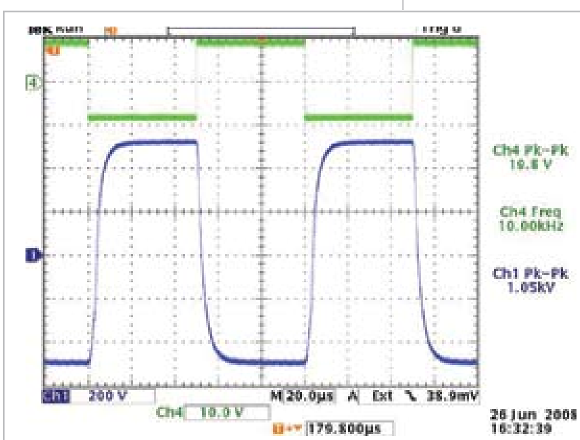

Figure 2 The amplifier's square-wave response at 10 kHz shows some high-frequency cutoff.

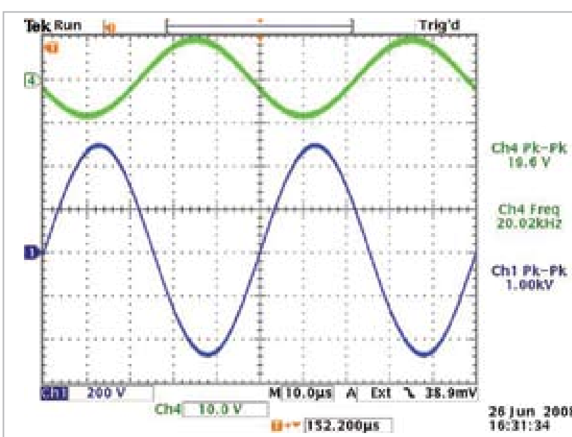

Figure 3 The amplifier's sine-wave response at 20 kHz shows a clean output signal.

sistors R_4 and R_5 provide the necessary bias to guarantee that the output transistors are always on. Careful trimming of R_4 and R_5 can remove the output crossover distortion. Zener diodes D_1 and D_2 keep the optoisolator photodiodes back-biased at 6.2V. Resistors R_{10}, R_{11}, R_{12}, and R_{13} supply some negative feedback to the output transistors. You must mount the four STW8N80 N-channel MOSFETs on suitable heat sinks to keep them cool. The circuit requires no active short-circuit protection. One pair of 125-mA currents across the high-voltage supply lines is sufficient to safeguard the circuit from destruction.

Figure 2 shows the square response at 10 kHz. There are no overshoots or undershoots, and the rising edge is almost antisymmetric with respect to the trailing edge. **Figure 3** shows the sine-wave response at 20 kHz. Both outputs are 1 kV p-p. EDN

DPGA conditions signals with negative time constant

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DPGAs (digitally programmable-gain amplifiers) amplify or attenuate analog signals, which maximizes an ADC's dynamic range. Most monolithic DPGAs, such as the Linear Technology (www.linear.com) LTC6910 and the National Semiconductor (www.national.com) LPM8100, use a multiplying DAC in an op amp's feedback loop so that the DAC's input code sets the amplifier's closed-loop gain. Instead of using a monolithic DPGA, you can use two op amps and three analog switches to build a DPGA employing negative time constants.

You're no doubt familiar with the $e^{-t/RC}$ convergent exponential in which a capacitor in an RC circuit asymptotically discharges to zero. For input voltage, $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V=V_{IN}/4$ at $t=2T$, $V=V_{IN}/8$ at $t=3T$, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). If you replace resistor R with −R, you create a positive RC time constant. Thus, you create a divergent exponential, $V_{IN}e^{+t/RC}$.

Instead of converging to zero, the waveform theoretically diverges to infinity, and $V=2V_{IN}$ when $t=T$, $V=4V_{IN}$ at $t=2T$, $V=8V_{IN}$ at $t=3T$, and so forth. Therefore, you can amplify the in-

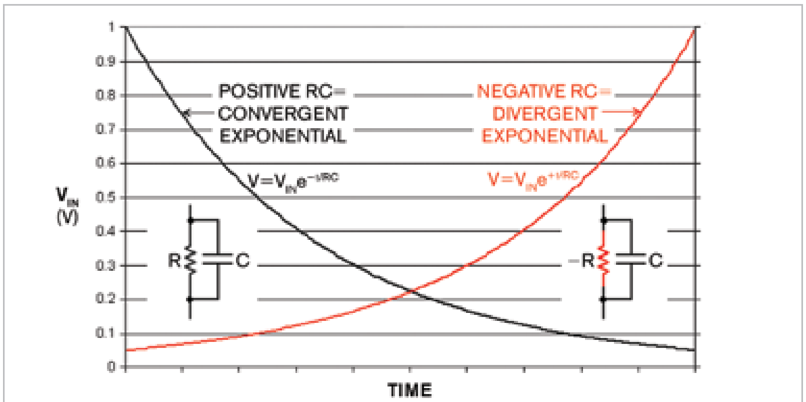

Figure 1 A negative time constant causes voltage to increase exponentially over time.

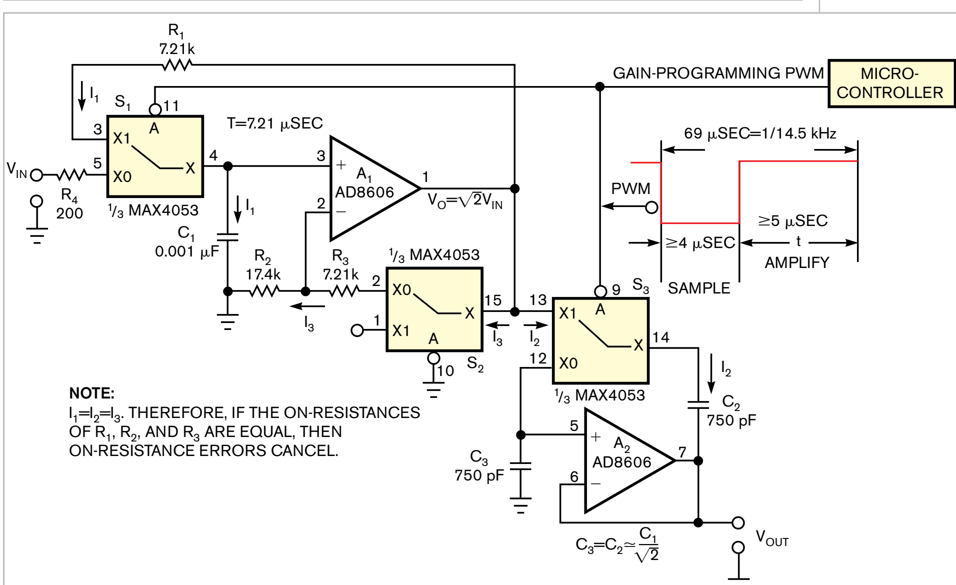

Figure 2 Positive feedback from amplifier A_1 causes C_1 to increase in voltage, which exponentially amplifies the input voltage.

put voltage by simply waiting the right amount of time ($t=\log_2(V/V_{IN})T$) after starting the negative discharge. The divergent exponential and the negative time constant are the core concepts of the circuit in **Figure 2**.

You can program the amplifier's gain with a PWM (pulse-width-modulation) signal from a microcontroller or another circuit. When the PWM signal goes to logic zero, sample-and-hold capacitor C_1 charges to V_{IN}. When the PWM signal cycles to logic one, op amp A_1 drives the R_1C_1 positive-feedback loop, creating a negative time constant. The resulting divergent exponential rise of C_1's charge continues as long as the PWM signal remains at logic one. That situation creates a net voltage gain of:

$$V_{OUT}(t)=V_{IN}2^{(t/10\ \mu sec+0.5)}.$$

THE NEAR-UBIQUITY OF PROGRAMMABLE-TIMER/COUNTER HARDWARE MAKES IT EASY TO DIGITALLY GENERATE A HIGHLY REPEATABLE PWM-CONTROL SIGNAL.

Thus, gain$=2^{(t/10\ \mu sec+0.5)}$ and log(gain)$=3+0.6$ dB/µsec. At the end of the amplification cycle, when PWM returns to logic zero, amplifier A_2 captures and holds the amplified input voltage.

The logarithmic relationship between gain and timing provides excellent gain resolution even when a PWM signal has just 8 bits of resolution and its programmable gain has a range greater than 0.2 dB/LSB step. (To view the log and linear plots of gain versus time using the amplify phase, go to the Web version of this Design Idea at www.edn.com/090319dia.)

The accuracy and repeatability of the timing of the exponential signal, the ADC sampling, the jitter, and the RC-time-constant stability all limit the amplifier's gain-programming accuracy. In **Figure 2**, 1 nsec of timing error, or jitter, produces 0.007% of gain-programming error. Fortunately, the near-ubiquity of programmable-timer/counter hardware in microcontrollers and data-acquisition systems usually makes it easy to digitally generate a highly repeatable PWM-control signal. **EDN**

Instrumentation amplifier compensates system offset from single supply

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Many integrated instrumentation amplifiers have architectures that permit offset compensation. The reference terminal's voltage, V_{REF}, adds in phase to the output to yield a gain of one. As a result, you can reset the output offset voltage by applying to the V_{REF} input a correction voltage of equal value but of opposite polarity. If the instrumentation amp operates from a dual-supply voltage, you can easily provide both positive- and negative-correction voltage. However, some instrumentation amps operate from a single supply—for example, in a battery-powered application—to amplify a signal source or a sensor that introduces a positive offset voltage. A sensor such as the AD590 from Analog Devices (www.analog.com), for example, produces an output current proportional to absolute temperature, and you should calibrate it at the lower reference temperature. In this case, the output swing of the instrumentation amp decreases, especially with high gain. To prevent this effect, you must apply a negative-correction voltage, which you generate from the positive power supply. In precision applications, the application of such a voltage may cause a problem.

This Design Idea shows you how to build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input. The circuit in **Figure 1** employs the dual high-precision OPA2333 op amp from Texas Instruments (www.ti.com). This op amp can

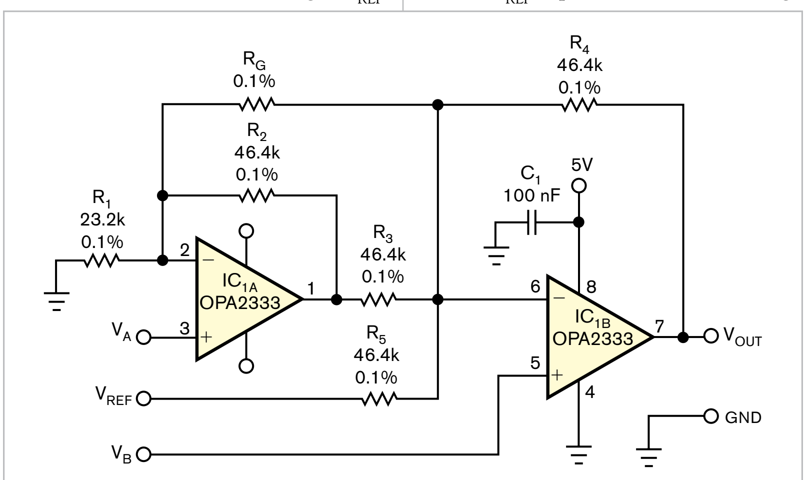

Figure 1 You can build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input.

operate from a 1.8 to 5.5V supply and uses a proprietary autocalibration technique to simultaneously provide a maximum offset voltage of 10 μV and near-zero drift over time and temperature. It also offers high-impedance inputs that have a common-mode range 100 mV beyond the supply rails and rail-to-rail output that swings within 50 mV of the rails. Applying the superposition of the effects to the circuit in **Figure 1** yields the following **equation**:

$$V_O = V_B\left[\left(1+\frac{R_4}{R_3\|R_5\|R_G}\right)+\left(\frac{R_4}{R_3}\right)\left(\frac{R_2}{R_G}\right)\right]-V_A\left[\left(1+\frac{R_2}{R_1\|R_G}\right)\left(\frac{R_4}{R_3}\right)+\left(\frac{R_4}{R_G}\right)\right]-V_{REF}\left(\frac{R_4}{R_5}\right).$$

To achieve equal gain for both the V_B and the V_A inputs, resistors R_2, R_3, R_4, and R_5 must have equal values that are double the value of R_1. Using the resistor values in **Figure 1**, you obtain the following simplified **equation**:

$$V_O=\left(3+\frac{92.8\ k\Omega}{R_G}\right)(V_B-V_A)-V_{REF}.$$

The amplifier's differential gain is $3+(92.8\ k\Omega/R_G)$, and the reference voltage is added, inverted together with the output signal. Resistor R_G sets the gain, and, if you do not connect R_G, the gain assumes the minimum value, which is three; decreasing the value of R_G to 93Ω increases the gain to 1000.

The V_{REF} input requires a low-impedance connection to preserve a good CMRR (common-mode-rejection ratio); otherwise, you can use an op-amp buffer for better CMRR, which depends mainly on resistor-ratio matching. In this implementation, to preserve an acceptable CMRR, you must use precision film resistors. Analyzing the circuit, you can calculate the worst-case CMRR at low frequency. With R_2, R_3, R_4, and R_5 all of equal value and double that of R_1 and with all the resistors having equal tolerance, you obtain:

$$CMRR=\frac{3+\dfrac{2R}{R_G}}{6\left(\dfrac{\Delta R}{R}\right)},$$

where ΔR/R is the resistor's tolerance. If the tolerance is 0.1% and with the minimum differential gain, which is three, you obtain a CMRR of at least 54 dB. With a differential gain of 100, you obtain a CMRR of at least 84 dB.

The V_{REF} input can reduce the system offset to the lower output-swing limit but does not reset it completely because, in that case, the output voltage would be unable to reach the single-supply ground. If you want instead to reset the output offset, you can subtract this value using an ADC with differential inputs (**Reference 1**).EDN

REFERENCE

1. Bruno, Luca, "Circuit compensates system offset of a load-cell-based balance," *EDN*, Aug 16, 2007, pg 71, www.edn.com/article/CA6466208.