

Teamwork makes challenging design task feasible

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By **Ron Wilson**, Executive Editor

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BILL VAILLANCOURT
SiGe Semiconductor

Entering the market for IEEE 802.11n Wi-Fi hardware in 2008 might seem like a questionable proposition in a market teeming with announced and hinted entrants. Entering with a separate RF-front-end module in a market in love with integration might also seem strange.

The design team from SiGe Semiconductor made

those moves, however, and with some solid reasons. If the team could manage a challenging design to requirements and schedule, the company believed it would have an advantage. Thus was born the design effort for the SE2593A module.

The advantage was simple: no process compromises. To hit the emaciated cost points necessary for commodity 802.11n access points and terminal cards and still achieve a near-zero board footprint, vendors had been making hard choices: How do we minimize the number of

semiconductor substrates? How do we achieve the lowest possible power? How do we slash the number of passive components? All of these questions have answers, but all usually mean compromises to performance.

A single-chip RF front end is certainly possible for an 802.11n radio, but each major component—the two power amplifiers at 2.4 and 5 GHz, the low-noise receiver amplifiers, the diplexers, and the transmitter/receiver switch—could ideally be in a different technology for optimum linearity, efficiency, and noise figures. Hence, any attempt to combine some of these components onto one die would risk performance compromises that might show up in field behavior.

SiGe’s design team decided to take on a challenge: producing a module that uses the best technology for each component but still remains cost- and footprint-competitive with more monolithic approaches. It would mean simultaneously managing several chip designs using different models and tool sets, pulling all

The SiGe team included (left to right) Paul Huang, Chris Masse, Tony Quaglietta, Michael Goss, Joe Soricelli, and Mark Doherty. Also on the team were Craig Christmas, Ted Whitaker, Adrian Long, Gord Rabjohn, Bill Vaillancourt, Ed Pierce, and Peter Gammel.



the results together into a module, and somehow controlling the size and cost.

An architecture

In a way, differentiating by optimal process choices came naturally. As the company's name suggests, SiGe Semiconductor has deep experience in, and affinity for, processes other than vanilla CMOS. In fact, a SiGe (silicon-germanium) BiCMOS (bipolar-complementary-metal-oxide-semiconductor) chip would become the center of the module design, implementing both the 2.4-GHz power amp and the control circuitry that provided a serial interface to the baseband processor and programmable bias to the 5-GHz power amp.

"We wanted to get as much as we possibly could into the less expensive SiGe process," explains Bill Vaillancourt, senior director of the computer and home-electronics group at SiGe. "That meant creating the bias voltages for the A-band amplifier on the SiGe die and then passing them across to the A-band die." It also meant implementing the power detector for both amplifiers on the SiGe die.

The team chose to implement the A-band amplifier in GaAs (gallium arsenide) and selected a PHEMT (pseudomorphic-high-electron-mobility-transistor) process for the low-noise amplifiers, diplexers, and transmitter/receiver switch.

It was feasible to fit all three dice into a 5×6-mm package. But there was the small problem of the passive components for the transmitter filters and other signal conditioning. For those parts, the designers turned to yet another technology, IPDs (integrated passive devices). Three IPDs would be expensive but potentially less so than the discrete passives they would replace. The designers combined this technology with a substrate carrying the signal routing and some additional passives. The package vendor would bond the dice and IPDs to the substrate and then wire-bond the contacts on those devices to the substrate-interconnect pads. Die stacking was not used because the 1-mm height requirement for the module made stacking impractical.

A design flow

The design would require a cross-section

of the company's resources, including teams in the United States, the United Kingdom, and Canada. Each chip design and the IPD work would require its own set of design tools and models. And the company's Hong Kong center, which manages assembly and test subcontractors, had to keep those teams in the loop, as well. Yet the company could not do the design in a piecemeal fashion. "We started from the pins of the module and worked our way in," says Vaillancourt. So, starting with the 50Ω signal connections and 3.3V supply, the design team proceeded to fill in the block diagram.

"It was absolutely necessary for everyone to have a good understanding of the design requirements from the beginning," Vaillancourt says. That foundation, plus regular meetings, frequent design reviews, and lots of conference calls, kept the three teams moving together. A specification doesn't cover everything, Vaillancourt points out. "You can't specify beforehand the isolation requirements on a die or the interactions between the transmit and receive chains. Everyone has to keep talking."

The key to the design process was extensive EM (electromagnetic) simulation. "We are used to having accurate EM models and simulating until the design is ready for tapeout," says Vaillancourt. "So, we applied that approach not only to the SiGe chip but also to all the chips." The continuous use of EM simulation was the best weapon the team had to control signal integrity. And, on such a dense module, signal integrity was a vital concern.

The team didn't just simulate the chips in isolation. "We never stopped cosimulation," says Chris Masse, the company's manager of module design. Working from the pins in, "the module design wrote the spec for the die designs. From there, we continuously refined the designs for the module, the dice, and the system in parallel."

SiGe had to do all of the detailed work for each die or IPD using the tool chain for that specific device. "It was a significant challenge working with different design kits and different tools for each technology," Masse observes. But all the information from the detailed simulations flowed into S-parameter models for system

simulation. At the system level, the team applied both functional and Monte Carlo analysis using linear simulation. Masse says that the company decided against using harmonic-balance techniques because simulation would have taken too long.

Even at the mechanical level, simulation proceeded from abstract models to details. Only fine details, such as wire-bond lengths—which in the end would depend on the assembly subcontractor's equipment—had to remain empirical.

And the results

The multitrack design flow did converge. The only significant disruption to the flow was a change in specifications. "Right in the middle of the design, customers told us we would have to use a halogen-free substrate for the module," Vaillancourt says. So, the team had to resimulate the whole system with a new substrate material.

"Fortunately, that [task] meant only a small shift in the dielectric constant for the substrate," adds Masse. "It wasn't a matter of redesign so much as determining how much detuning the new material would cause and what that [detuning] would cost us in yield. We ended up touching a few of the traces to recenter the design a bit."

The largest unknown throughout the design was not even in the module; it was in the operating environment. "The typical Wi-Fi card is a horrible environment for RF," Vaillancourt observes. "In a MIMO [multiple-input/multiple-output] configuration, you need very linear behavior from your power amps at both full power and backed-off. ... You have to build in enough programmability to adapt to the uncertainties in the customer's design."

By providing programmable bias points and 50Ω connections to the outside world, the design team hoped to minimize the customer-support problem. And, if problem reports are a measure of success, the team seems to have succeeded on all fronts. "Customer boards came up very quickly with the sample modules," Vaillancourt reports. "With the sample board layouts, the data sheet, and the compliance matrices we are providing, we actually need very little applications-engineering engagement on our customer sites." ■