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Selecting the correct process geometry and options

Most of the custom chips today, including ASICs, ASSPs (application-specific standard products), and special-purpose custom chips, have function blocks that do not require leading-edge processes. This situation has introduced the task of selecting which process node is the most appropriate for the design opportunity. The traditional metric for process selection is the speed requirement for the logic and the associated pin-to-pin clock rate. These criteria determine the minimum device geometry, the junction profiles, the number of layers of interconnect—which in turn determines the areal density of gates—and the type of substrate material. Most of the digital-only designs with fewer than 100 million gates use these criteria, and they work well.

Most new designs, however, incorporate more than just high-speed digital logic. Memory options, analog and mixed-signal blocks, and packaging and assembly options have now become critical factors in the fabrication-process selection. Power consumption is also a major factor in identifying an appropriate process node. As designers evaluate older processes, they must be aware of the intended operating voltage of the design as well as the threshold-voltage selections that are available.

Some older processes, particularly in mixed-signal devices, can support operation at a voltage as high as 12V with 0.7V threshold voltages. These processes may not be appropriate choices for a design aiming for 1.2 to 1.3V operation. Conversely, some nominally 3.3V-sensor applications may not work well with 65- or 45-nm technologies that are using 0.3V thresholds and device-breakdown voltages of 2.7V.

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Some of the common high-volume processes, such as 180, 130, and 90 nm, are available in multiple process options. These options include standard logic, mixed-threshold logic, analog with special resistors and capacitors, RF with inductors and special FETs, high-density memory, and low-power and low-leakage process flows. Each of these options has a unique set of device models, design rules, layer lists, and IP (intellectual-property) libraries. The design blocks are not generally interchangeable among the processes. It is important that designers observe which option their teams have selected and which rules and device types apply to those designs and processes.

One area of misunderstanding in process selection lies in the interconnect and passivation, or back-end-of-line-flow, options. Processes of 0.25 micron and larger generally use only aluminum interconnect with a bimetal plug implant. Geometry processes at 130 nm and smaller usually use copper-only interconnect. Processes in the midrange, such as 150, 180, and 200 nm, support either all-aluminum interconnect, all-copper interconnect, or a mix of both. The selection of the interconnect can determine whether a focused-ion-beam tool can work on and repair the design. It can also influence the effectiveness of multilayer probing using an e-beam and what postprocessing, including thin film and other material deposition, is possible.

Most of the new bioelectronics chips and a number of the integrated MEMS (microelectromechanical-systems), sensors, and electronics designs require postprocessing steps. Many of these designs use specialty thin films and polymer-based films on the surface of the die, and these films require direct contact with the active circuitry at the metal, polysilicon, or diffusion layer. As a result, designers must carefully plan the use of metal fill, fill-blocking mask, and low-k dielectrics to accommodate contact with the thin-film layer in the postprocessing flow. Most of the etch steps for these deposition layers to contact the inner layers of the die are nonstandard and, thus, may alter the electrical performance of the design.

When selecting a process, designers must address these issues as well as backside-wafer processing, including etch, etch and gold, and "backlapping" to thin the wafer. It's not just about logic performance. EDN

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