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Endpoint distortion

Figure 1a and Figure 1b depict two common transmission-line scenarios: series termination and end termination, respectively. Both drivers are fast with negligible series output resistance. The capacitive loads represent the input capacitances of the CMOS receivers. In the series-terminated case, a step edge from the driver proceeds to the right, interacts with the load, and reflects back toward the driver. The capacitive load may create a strange-looking reflection, and it may distort the appearance of the

received signal, but whatever bounces off the load returns to the driver termination and dies, never to be seen again. As a result, the receiver sees one step edge, possibly distorted but with no lingering aftereffects. Of all the things that could go wrong with a circuit, this distortion is not too bad.

Figure 1 illustrates an equivalent-endpoint circuit that defines the nature of instantaneous signal distortion at the receiver. The equivalent circuit comprises two components: a series resistance equal to the line impedance, and a shunt capacitance representing the input capacitance of the receiver (Reference 1).

The RC lowpass filter thus formed

disperses the input rise time. It also delays the signal's time of arrival by an amount equal to the group delay of the filter, in this case $Z_0 C_{IN}$.

If your native signal rise or fall time is much faster than $Z_0 C_{IN}$, then the filter slows the signal edge to the point where it mimics the filter step response—a nice, clean rising edge with a 10 to 63% rise time of $Z_0 C_{IN}$. If, on the other hand, your native signal rise or fall time is slower than $Z_0 C_{IN}$, the filter has little effect. If you look closely, however, you will see that the filter delays the time of arrival of the signal's midpoint by the amount $Z_0 C_{IN}$.

In Figure 1b, a parallel combination of the transmission line and the

end termination feeds the capacitive load. If the end termination is properly set equal to Z_0 , the parallel combination must be less than Z_0 , so the load in this case responds more quickly, causing less distortion than in the series-terminated case.

If the PCB (printed-circuit-board) trace delay is longer than the signal's rise or fall time, the effective impedance at the end of the trace, which you measure on a scale of time commensurate with one rising or falling edge, equals simply Z_0 . In that case, the parallel impedance driving the capacitor is $(1/2)Z_0$, and the time constant associated with the RC filtering effect is $(1/2)Z_0 C_{IN}$, half that of the series-terminated case. On the other hand, if the PCB trace delay is shorter than the signal rise time, the effective impedance at the line's end decreases as it becomes a mixture of the driver and the line impedances, even further reducing the time constant.

The good news is that end terminations respond quickly. The bad news is that the capacitive load degrades the performance of the end termination. Upon receipt of each signal edge, the degraded termination reflects a short pulse back toward the driver. The driver has no termination, so it reflects the pulse a second time. The end of the line thus receives an initial distorted signal edge followed one round trip later by a small reflected pulse.

When signal timing fidelity is of utmost importance, the end-terminated architecture provides the least rise-time dispersion and variation in timing in response to variable load capacitance. In exchange for its improved short-term response, the end termination suffers the possibility that round-trip reflections will interfere with subsequent bits. **EDN**

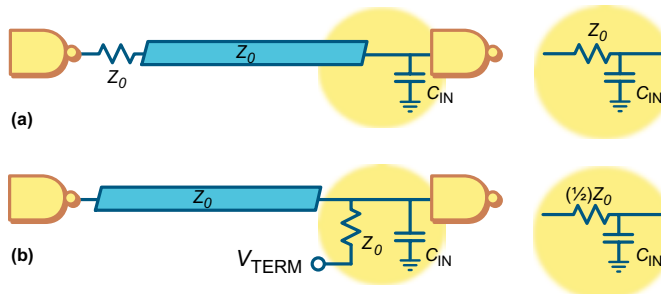


Figure 1 All PCB nets suffer endpoint distortion. Two common transmission-line scenarios are series termination (a) and end termination (b).

REFERENCE

1 Johnson, Howard, "Driving-point impedance," *EDN*, May 14, 2009, pg 12, www.edn.com/article/CA6656309.