



BY BONNIE BAKER



Is your amplifier offset way out of whack?

Have you ever spent a great deal of time selecting the perfect operational amplifier for your circuit, only to find that the offset voltage is wrong at the manufacturer's bench-specified input? What if you find that it is more than 10 times higher than specification in your application circuit? Do you send the chip in for failure analysis or just toss the chip out and have another look at your list of amplifiers? As an alternative, I suggest that you try to explain the offset error by re-examining your amplifier's specifications.

If you are using your amplifier as the key component in a transimpedance amplifier, an analog filter, a sample-and-hold circuit, an integrator, a capacitance transducer, or any other circuit with high-impedance components around your amplifier, you might find that the amplifier's input-bias current creates an offset-voltage error through the resistors in your circuit.

In the bipolar-amplifier days, the term "input-bias current" was an accurate descriptor, and it still is. A bipolar amplifier's input-bias current is the

same as the base current of the NPN or PNP transistors at the input of the amplifier. The magnitude of the bipolar amplifier's input-bias current ranges from a few nanoamperes for low-power devices to hundreds of nanoamperes for higher-power devices.

The term "input-bias current" loses its meaning when you look at JFET or CMOS input amplifiers. With these types of amplifiers, the current sinking or sourcing from the amplifier's input pins is actually the leakage current from the input-ESD (electrostatic-dis-

charge) cells (Figure 1). A more accurate descriptor for this current error is "input-leakage current." The magnitude of leakage current with JFET or CMOS amplifiers is less than 1 pA at 25°C. This specification is independent of the common-mode voltage and the magnitude-amplifier power. Almost all amplifiers have ESD cells for protection from an ESD event, but you will never see ESD-leakage current in bipolar amplifiers. The input-bias current swamps out the picoampere leakage current from the ESD cells.

Input-bias and input-leakage current can change over temperature. However, depending on the operational-amplifier design, the bipolar input-bias current can be fairly stable. The JFET and CMOS input amplifiers may not be, however. Because the leakage current is from the reverse-biased ESD diodes, the leakage current increases approximately two times per 10°C change.

In ensuring that the input-leakage current remains low with JFET and CMOS amplifiers, you must understand the impact of your PCB (printed-circuit board) on the picoampere levels of current. For instance, a small amount of dust, oil, or water molecules can increase leakage current and masquerade as input-bias current. The good news is that, if you exercise special care, you can build a PCB that will adhere to a 1-pA performance specification.

The most effective way you can reduce or minimize the effects of input-bias or input-leakage current is to check your circuit configurations. As you examine your circuits, look at the voltage characteristics of each node and make sure that you understand the impact of all of the current paths in your circuit. **EDN**

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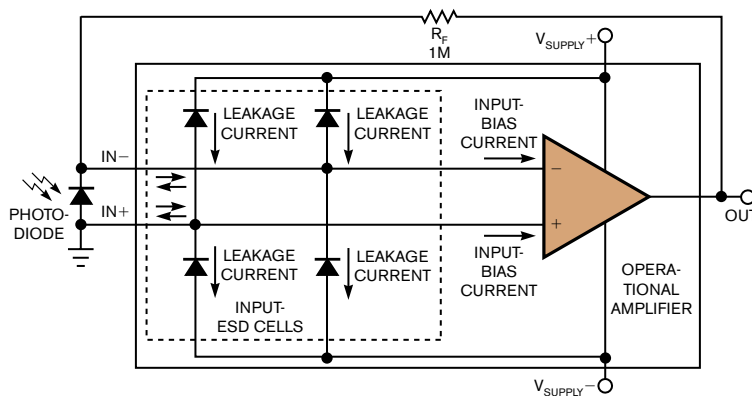


Figure 1 Input-bias or -leakage current creates a voltage drop across R_f .