



BY HOWARD JOHNSON, PhD

Holding on

Switch the CMOS-driver model high in **Figure 1** by closing S_1 and opening S_2 . Wait for the line to settle. Because there is no dc load—only capacitance—the steady-state current equals almost zero. It differs from zero only according to the tiny leakage currents associated with the driver, the receiver, and the transmission line itself.

After settling, if you tristate the driver by opening S_1 , the line remains in its high state, drifting slowly according to the leakage.

In practical terms, you can sometimes obtain many nanoseconds of dependable storage time in the tristate mode. The tristate feature, if available in your driver, acts as a sort of additional short-term dynamic-memory element that you can use to extend the hold time of your driver. It is just as reliable as any other DRAM circuit because it uses the same principle. The

main difficulty is obtaining reliable information about the worst-case leakages. If you want to test the leakage, remember that leakage in the driver circuit grows exponentially with temperature, so test the circuit when it's hot.

The following example illustrates a situation in which a tristate technique might be helpful. Imagine two synchronous master-slave latches that the same 10-MHz synchronous clock drives. One, D_{OUT} , feeds data to the other. They both operate on the positive clock edge. At that speed, assum-

ing modern CMOS logic, the circuit probably enjoys plenty of setup-timing margin but may lack hold margin, especially if the first device is much faster than the second.

The receiving latch may require more hold time than the transmitting latch guarantees. To expand the hold time on D_{OUT} , you may delay the clock feeding the transmitting device, insert a delay in series with the transmitted datapath, or invoke the tristate condition on the transmitter for a brief interval before and after each clock edge to prevent the output from changing until the required hold time for the receiving latch expires. Note that the output goes tristate when the control signal is high.

Before disabling the output, you must wait for the line to settle completely. Should the device enter the tristate condition while the line harbors any significant reflections, those reflections will bounce off C_{OUT} at the driver and C_{IN} at the load, and they thereafter ring back and forth in a highly resonant fashion. The residual ringing may persist into the critical timing zone. The source termination cannot prevent that type of ringing, not even if it is a perfectly laser-trimmed polysilicon resistor, because, during the tristate condition, the resistor no longer leads through a closed switch to a low-impedance power rail. It just leads to C_{OUT} . The source resistor works as a termination only when the driver is enabled. As a result, you must first wait for the line to settle and then invoke the tristate mode.

In some circumstances, tristating a line can exacerbate your difficulty with crosstalk or susceptibility to ESD (electrostatic discharge). Check for those conditions when the driver is active and when it is in the tristate condition. **EDN**

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com.

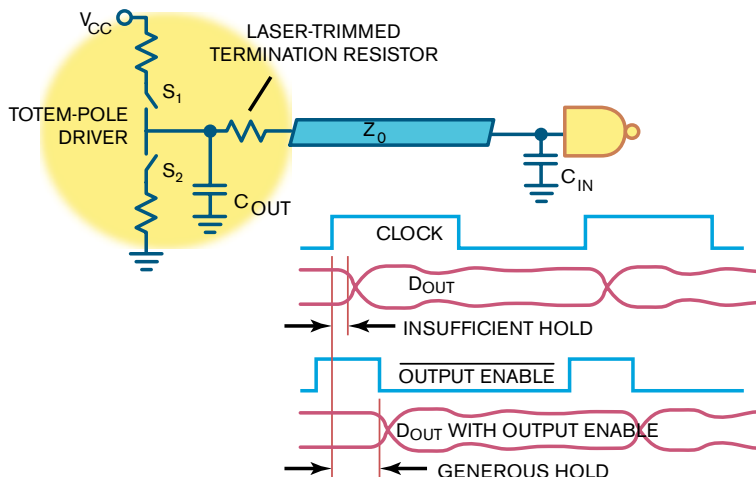


Figure 1 Clever timing can extend the D_{OUT} hold time.