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Using an analog filter to inject noise

Sometimes things just don't make sense! For instance, your RC filter or amplifier's lowpass filter at the input of a delta-sigma ADC can produce a noisier digital output. Didn't you design the filter to reduce noise so that you'd get more instead of fewer noiseless bits from your converter? It is as easy to eliminate higher-frequency noise with an analog lowpass filter as it is to inject noise into the frequency band below the corner frequency of your filter. If your filter produces noise in the frequency band of interest, your conversion output results will be noisier than you might expect.

If you change your circuit design by reducing your filter's resistor values, you will increase the noiseless bits in the circuit. For example, the delta-sigma ADC in **Figure 1** uses a lowpass filter to reduce noise above the converter's output data rate, F_D . With this filter, use the output data rate of the

delta-sigma converter to select the resistor and capacitor values in this circuit. You can use the formula $F_D = 1/(2\pi R_{FLT} \times C_{FLT})$ to calculate the values of R_{FLT} (filter resistance) and C_{FLT} (filter capacitance). This filter reduces noise by targeting the sampling frequency of the converter as the combi-

nation of $R_{FLT}/2$ and C_{FLT} goes to work (**Reference 1**).

The missing detail in this design formula is resistor noise. There is no such thing as a noiseless resistor. The ideal resistor noise is $\sqrt{(4 \times k \times T \times R \times B)}$, where k is Boltzmann's constant ($1.38 \times 10^{-23} \times \text{JK}^{-1}$), T is the temperature in Kelvin, R is the nominal resistance in ohms at 25°C, and B is the bandwidth of interest in hertz.

Now, let's make sense of this resistor-noise formula. The noise that you inject into your circuit up to the output data rate is equal to the resistor noise. To determine the maximum allowable resistance value in this circuit, use the following **equation**:

$$R_{FLT(MAX)} = \frac{10^{-(ER \times 0.602)}}{4 \times k \times T \times F_D}$$

where ER is the specified effective resolution from the ADC manufacturer's data sheet. **Figure 1** illustrates the characteristics of this formula. If you operate your 23-bit-effective-resolution delta-sigma converter at a data rate of 200 Hz, the maximum value of the filter's resistance is 4.297 kΩ or less, and $R_{FLT}/2$ is 2.148 kΩ or less. **EDN**

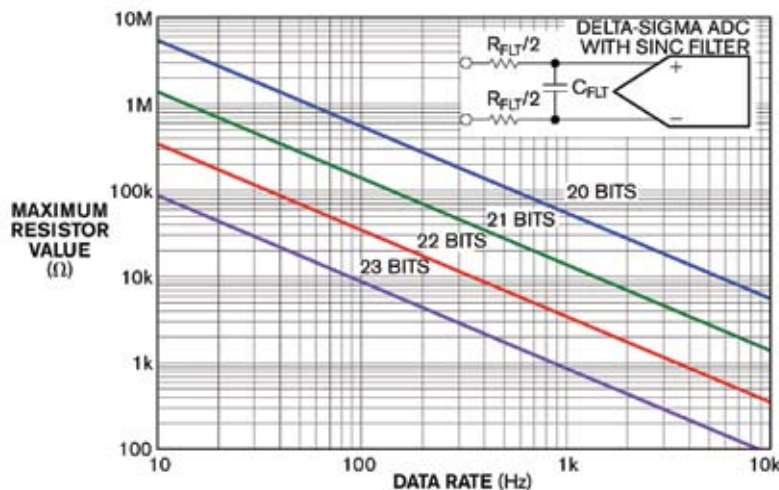


Figure 1 The combination of $(R_{FLT}/2 + R_{FLT}/2)$ and C_{FLT} reduces circuit noise as long as the filter's resistance noise is below the ideal converter's noise.

REFERENCES

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