

“Dog” PLL chases its own tail



Long ago, I was developing experimental LAN-interface hardware to transmit data on a synchronous-RF carrier from a master unit to remote devices that simultaneously returned data on a synchronous-RF carrier two octaves lower. I amplified the received carriers to TTL (transistor-transistor-logic) levels for digital-PLL (phase-lock-loop) CDR (clock and data recovery).

One of the biggest problems was getting the master unit's receiver PLL to recover the returned carrier without jittering all over the place when the loop-filter bandwidth was small. No matter what I tried, the LC (inductor/capacitor) oscillator on the wire-wrapped breadboard simply would not run in a stable fashion at a narrow loop bandwidth. It insisted on wild phase gyrations around the phase-lock point.

I suspected that synchronous digital noise from both the local transmitting oscillator and returned carrier was pulling the PLL oscillator. I verified this suspicion by disconnecting the PLL-control voltage from the oscillator varactor, leaving only the assumed stray noise

coupling. Sure enough, when I manually tuned the oscillator close to the operating frequency, the device locked strongly and stably to the digital noise without jitter.

Rebuilding the LC oscillator in a metal box to fully shield it from digital electromagnetic fields and filtering the power-supply- and control-voltage inputs resulted in an amazing improvement. I learned that you must protect PLL oscillators from digital-synchronous-noise influences from supply rails and stray electromagnetic coupling.

About a year later, I was developing hardware that exchanged data between a remote slave and a master unit using two optical fibers. I had designed my receiver's clock recovery for both the

slave and the master to rely on well-behaved LC tanks rather than ornery PLLs. A colleague, on the other hand, had designed the master unit's optical-link clock generator to use a PLL digital IC with an RC (resistor/capacitor) oscillator. The master clock rate was 16.384 MHz, but the optical links required 19.456 MHz for pattern-synchronization overhead, and the budget did not allow for a more stable VCXO (voltage-controlled-crystal oscillator).

The optical link's transmitter PLL insisted on doing those wild phase gyrations. "Impossible," I thought. All noise transients from digital transitions occur just after the master oscillator's switching transition, so, in theory, it should not be susceptible to its own noise, but it was. Disabling the master's remote-unit receiver allowed the PLL to run stably and verified the cause of the problem: Its own stray digital noise was returning to haunt it through the long path to the remote unit and back again. This round-trip delay was unpredictable; every 10m of cable length was equivalent to a 360° shift in returned noise relative to the clock period. Because the oscillator was divided by 19, phase detection occurred only once every 19 clock cycles. In the intervening cycles, the oscillator was free to become a happy wanderer. With the remote unit 1 km away, the oscillator was tracking the influence of its phase from 10 μ sec and 200 clock periods earlier. This PLL was chasing its own tail.

We tamed the problem by building the VCO on a small PCB (printed-circuit board) with an unbroken bottom ground plane supported on a standoff above the main PCB. The oscillator's PCB ground plane helped to shield the topside circuit from the evil digital influences below. **EDN**

REFERENCE

■ Rabinovich, Rick, "Power-rail filtering improves PLL performance," *EDN*, March 19, 2009, www.edn.com/article/CA6645280.

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