



BY RON WILSON, EXECUTIVE EDITOR

SOI Industry Consortium stalks the “green thing”

In these days, only government spending seems to drive the economy, and everyone is lining up to be under one of those government spigots. This situation is tricky for the semiconductor industry because it's hard to make a case for a fabless semi company as being essential to bailing out Morgan Stanley, rebuilding our highway infrastructure, or checking the spread of swine flu. However, there is one area—energy saving—in which chips and foundries can claim some home turf.

Accordingly, just about half of new marketing programs have the word “green”—frequently capitalized—somewhere in the first paragraph of their promotional materials. Often, this approach is little more than spurious: an amplified echo of last year's key phrase, “low power.” In some cases, though, the appeal to “greenness” makes sense, even without adding chlorophyll to the package epoxy.

One such situation is a new initiative—“Simply Greener”—by the SOI (silicon-on-insulator) Industry Consortium (www.soiconsortium.org). Part of the point is to hitch SOI to the green bandwagon. But there's content in there, too: One of the significant advantages of SOI is its ability to deliver a better speed-power product on a given project than a similar-geometry bulk-CMOS design. Some of the more prominent press coverage of SOI—AMD's travails and the heat problems with industry-leading game consoles, for example—may have obscured this fact. Nonetheless, it is true.

The SOI folks want to make clear the point that you can use that speed-power-product advantage to save significant power at the same speed. To



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underline that fact, a recent presentation gives examples of benchmark tests from ARM and IBM, which show side-by-side designs of blocks in SOI and in bulk CMOS. In ARM's case, a 45-nm-datapath design, the SOI version achieved an almost-threefold reduction in leakage and an approximately 20% reduction in dynamic power. IBM's example was more apples-to-oranges: a full-chip migration from 65-nm bulk CMOS to 45-

nm SOI, resulting in an approximately one-third reduction in power and a 50% speedup. In these instances, the choice of SOI instead of the bulk process appears to be making more difference than the use of aggressive power management.

The mechanism for the efficiency gain seems to be simple—probably simpler than it actually is. Because SOI builds its transistors directly over a buried insulating layer, the parasitic capacitances from the source, drain, and channel are much less than in a bulk wafer. By reducing these capacitances, a SOI transistor can operate with lower drive current and, hence, can be smaller; have a higher threshold voltage; or offer both features. Thus, both leakage and dynamic currents can be smaller at the same performance level.

A second point the SOI Consortium wants to emphasize is that SOI is available as an off-the-shelf foundry process, not just as a full-custom technology. “There's a wide range of regular users now,” says Horacio Mendez, executive director of the consortium. “Almost everything IBM is building at 45 nm is in SOI, as are all of Freescale's latest networking chips. Casio is using the technology at extremely low power levels for watches, and some vendors are applying the technology in automotive applications.” Foundry service is available from IBM and Chartered Semiconductor, among others.

SOI not only is a viable option for ordinary design teams but also has a road map, the organization claims. Processes are available in 65 and 45 nm, and both 32- and 22-nm processes are on the drawing boards. The main ideas the consortium wants you to know are that SOI brings built-in power savings, and it is mainstream. Those points deserve some discussion, even from teams that are tooling up to work on bulk CMOS. **EDN**

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