

Unused port adds a PWM/analog channel to a microcontroller

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Low-cost, 8-bit, single-chip microcontrollers are stingy when it comes to on-chip PWM (pulse-width-modulation) resources. The use of a PWM resource often forces a de-

signer to sacrifice a capture/compare or timer channel because the PWM channel shares the same on-chip hardware. This Design Idea describes how you can use an on-chip unused synchro-

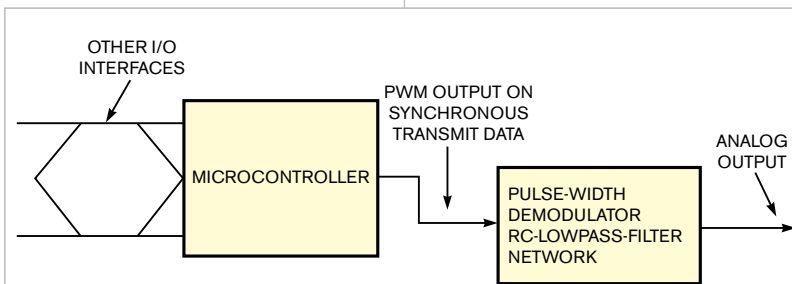
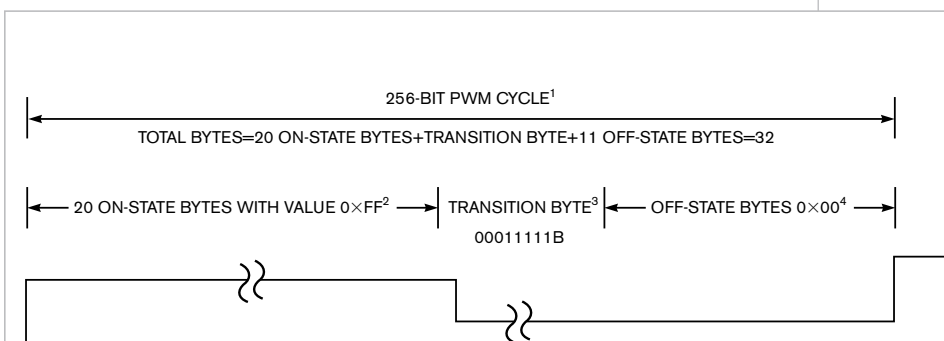


Figure 1 You can use an on-chip unused synchronous serial port to generate PWM signals and convert them to a slow-moving analog signal.



¹RAW DATA=165; ON-STATE=5V; OFF-STATE=0V.
²NUMBER OF ON-STATE BYTES=165/8=20 (INTEGER DIVISION).
 REMAINDER=165 - (8×20)=165 - 160=5.
³TRANSITION BYTE=00011111B=0×1F (NOTICE FIVE ONES FROM LSB SIDE).
⁴NUMBER OF OFF-STATE BYTES=TOTAL 32 BYTES - ONE TRANSITION BYTE
 - 20 ON-STATE BYTES=32 - 1 - 20=11 BYTES.
 ANALOG OUTPUT AFTER LOWPASS FILTER=(165/256)×5=3.22V.

Figure 2 You can generate raw data with a decimal value of 165 using this concept.

DIs Inside

44 Capacitance meter uses PLL for high accuracy

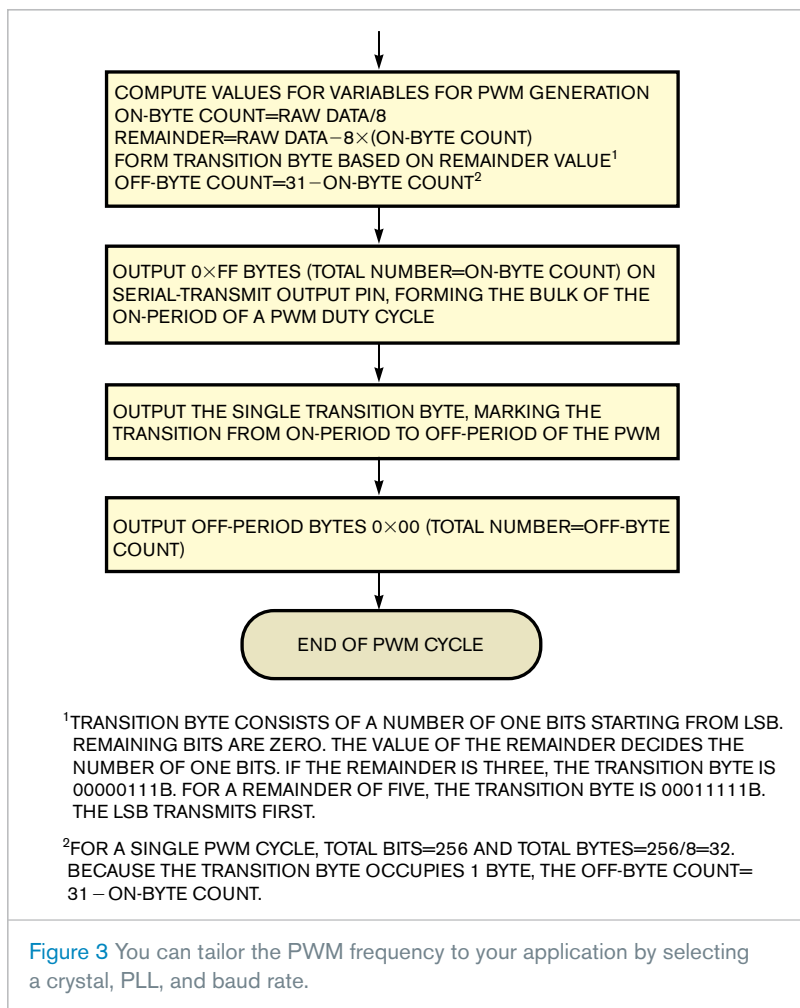
50 Resistor compensates for instrumentation-amp gain drift

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nous serial port to generate PWM signals and convert them to a slow-moving analog signal (**Figure 1**). Many microcontroller-based stand-alone electronic units don't use the synchronous serial port. Thus, you can use the microcontroller's baud-rate generator and parallel-to-serial-converter blocks to generate bit patterns to form a 256-bit PWM pattern. You can then filter the PWM output with an RC filter to extract an analog signal (**Reference 1**).

The synchronous communication is devoid of the start and stop bits of asynchronous mode, so the bit pattern can generate long periods of high or low level.

You can generate raw data with a decimal value of 165 using this concept (**Figure 2**). A PWM-conversion cycle consists of generating 256 bits—that is, 32 bytes. The number of "on" bits corresponds to the value of the raw data to convert into PWM. Hence, for 165 bits as the raw data, 165 bits are on and 91



bits are off. To generate a 165-bit on-period, the first 20 bytes—that is, 160 bits—transmit as 0xff on-state bytes. The trick lies in judiciously compos-

ing the 21st, or transition, byte. This byte has some of its LSBs (least significant bits) as ones and the rest as zeros to form the required length of the on-

period. In this case, the circuit needs five more on bits: $160+5=165$. Hence, the transition byte should have a 00011111b pattern (byte=0x1f).

Figure 3 illustrates the process in flow-chart form. You can tailor the PWM frequency to your application by selecting a crystal, PLL (phase-locked loop), and baud rate. A simple RC filter can convert the PWM into a slow-moving analog value. Although this idea describes an 8-bit PWM, you can increase or decrease resolution by changing the total bits per PWM cycle. You correspondingly increase or decrease the conversion time.


Listing 1, which is available at www.edn.com/091008dia, provides a sample code for illustrating the concept. The code uses the Microchip (www.microchip.com) PIC18F4525, which has a 4-MHz crystal and 10-kHz baud rate for the synchronous serial communication, yielding $10,000/256=39.31$ Hz of PWM frequency. You can filter it with a 0.1-sec RC filter, which is sufficient for slow-moving analog signals, such as speed setpoints for motion-control applications. By using a 20-MHz crystal, you can achieve synchronous serial baud rates greater than 1.5 MHz and PWM frequencies of a few kilohertz. **EDN**

REFERENCE

■ Mitchell, Mike, "Make a DAC with a microcontroller's PWM timer," *EDN*, Sept 5, 2002, pg 110, www.edn.com/article/CA240913.

Capacitance meter uses PLL for high accuracy

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 An old *Electronics Designer's Casebook* described a circuit that provided capacitance measurements of 10 pF to 1 μF with 1% accuracy (**Reference 1**). A number of issues emerged with the circuit during testing, and this Design Idea describes an improved circuit. The meter circuit in **Figure 1** (pg 48) lets you measure capacitance from

10 pF to 10 μF with high accuracy. It needs no microprocessor; thus, it needs no code. Even in the 1- to 10-pF range, the circuit is accurate to about ± 1 pF when reading values as low as 5 pF.

The circuit requires a high-input-impedance device to interface with the high-value resistors, R_6 , R_8 , R_9 , and R_{10} , and a fast comparator to interface

with the PLL (phase-locked loop). IC₁, an Analog Devices (www.analog.com) AD8033 op amp, does the job because of its 1000-GΩ input impedance and 1.7-pF input capacitance. It also has only 50 pA of input bias current over temperature. Its 80-MHz bandwidth and 80V/μsec slew rate are more than enough for this application. It can operate with just an 8V power supply. Unfortunately, the AD8033 is available only in surface-mount packages, which makes breadboarding somewhat tedious. IC₂, an Analog Devices ADCMP601 comparator, interfaces

with the AD8033 op amp and IC₃, a 74HC4606A PLL. The comparator has a typical propagation delay of only 4.3 nsec. It has built-in hysteresis and needs only a 5V supply. It is also available only in surface-mount packages.

The capacitance meter generates two signals; one of them lags the other by 60°. A 3-bit, self-correcting, divide-by-six twisted-ring counter comprising IC₆, IC₇, and IC_{13B} provides the lagging signal. The lagging signal connects to the COMP input of the PLL (Pin 3), and the other signal is applied to an RC circuit, which provides a 60° phase lag before it gets to the SIG input of the PLL (Pin 14). The PLL adjusts the frequency of its VCO (voltage-controlled oscillator) so that the two input signals are in phase. The resulting period of the VCO's output signal (Pin 4) is proportional to the measured capacitance.

On the low-capacitance range, signals with frequency F_O are applied to the PLL. On the high-capacitance range, the frequency is F_O/1000. IC₈ through IC₁₀ provide the division, and S₂, IC_{4B} through IC_{4D}, IC_{5D}, IC_{5E}, and the associated components provide the high-capacitance/low-capacitance range switching. The VCO of the PLL runs at 6F_O. The circuit divides this signal by three to provide an output with a period that's proportional to the measured capacitance. It provides the correct digits when you measure with a frequency counter that you set to measure the period. You can calculate F_O or F_O/1000 from 0.1505/R_XC_X, where R_X is R₆, R₈, R₉, or R₁₀, depending on the selected range.

The 74HC4046A PLL can exhibit several problems. For example, it may not start when you apply power, or it may hang with the VCO running with the VCO input pin (Pin 9) stuck high or low. The start-up circuitry,

comprising IC_{13F}, Q₄, and associated components, applies a positive voltage of approximately 2V to the VCO's input, which forces the VCO to oscillate. After the VCO starts, D₄ becomes back-biased, which disconnects the start-up circuitry from the VCO's input pin. If the VCO is running but hung with its input stuck high or low, one-shot IC_{12A} detects that it's not phase-locked by responding to pulses

THE 74HC4046A PLL MAY NOT START WHEN YOU APPLY POWER.

from Pin 1 of IC₃. The one-shot then issues a 1.5-sec pulse that causes IC_{12B} to produce a 0.5-sec pulse that causes either a positive pulse at the inhibit pin or a low pulse at the VCO's input pin, depending upon whether the PLL is low or high. After the 0.5-sec pulse ends, the pulse from IC_{12A} continues for 1 sec, giving the PLL time to lock. LED D₇ indicates phase lock. If the PLL phase locks, all is well. If it does not, the IC_{12A}/IC_{12B} one-shots continue issuing pulses. Experiments determined these methods for recovering from the anomalous states. It's possible that the circuit won't always recover, but these methods have been effective on the test unit.

The circuit applies the 6F_O signal, divided by three, to buffer IC_{5F}'s Pin 5. This action provides an output frequency whose period is proportional to the value of the measured capacitance. The output provides the correct digits without regard to the location of the decimal point. To determine the value of the unknown capacitance, observe the setting of S₁ and S₂.

You can calibrate the circuit by us-

ing a capacitance of a known value of approximately 1000 pF, with S₂ at the low-capacitance position and S₁ at the 100- to 1000-pF/0.1- to 1-μF position. Set R₂₂ at its midposition, connect a frequency counter to Pin 6 of IC_{3F}, and set the meter to measure the period of the signal. Adjust R₁₂ for a period whose digits agree with the known value of capacitance. Next, use a capacitance of approximately 100 pF and set S₁ to the 10- to 100-pF/0.01- to 0.1-μF position. Record the measured value of the capacitor. Then, using the same capacitance of approximately 100 pF, set S₁ to the 100- to 1000-pF/0.1- to 1-μF position and adjust R₂₂ to get the same value as you obtained on the 10- to 100-pF/0.01- to 0.1-μF position. The R₂₂/C₁₃ combination provides a small variable delay relative to the signal at Pin 14 of IC₃. This fine adjustment improves accuracy in the lower range.

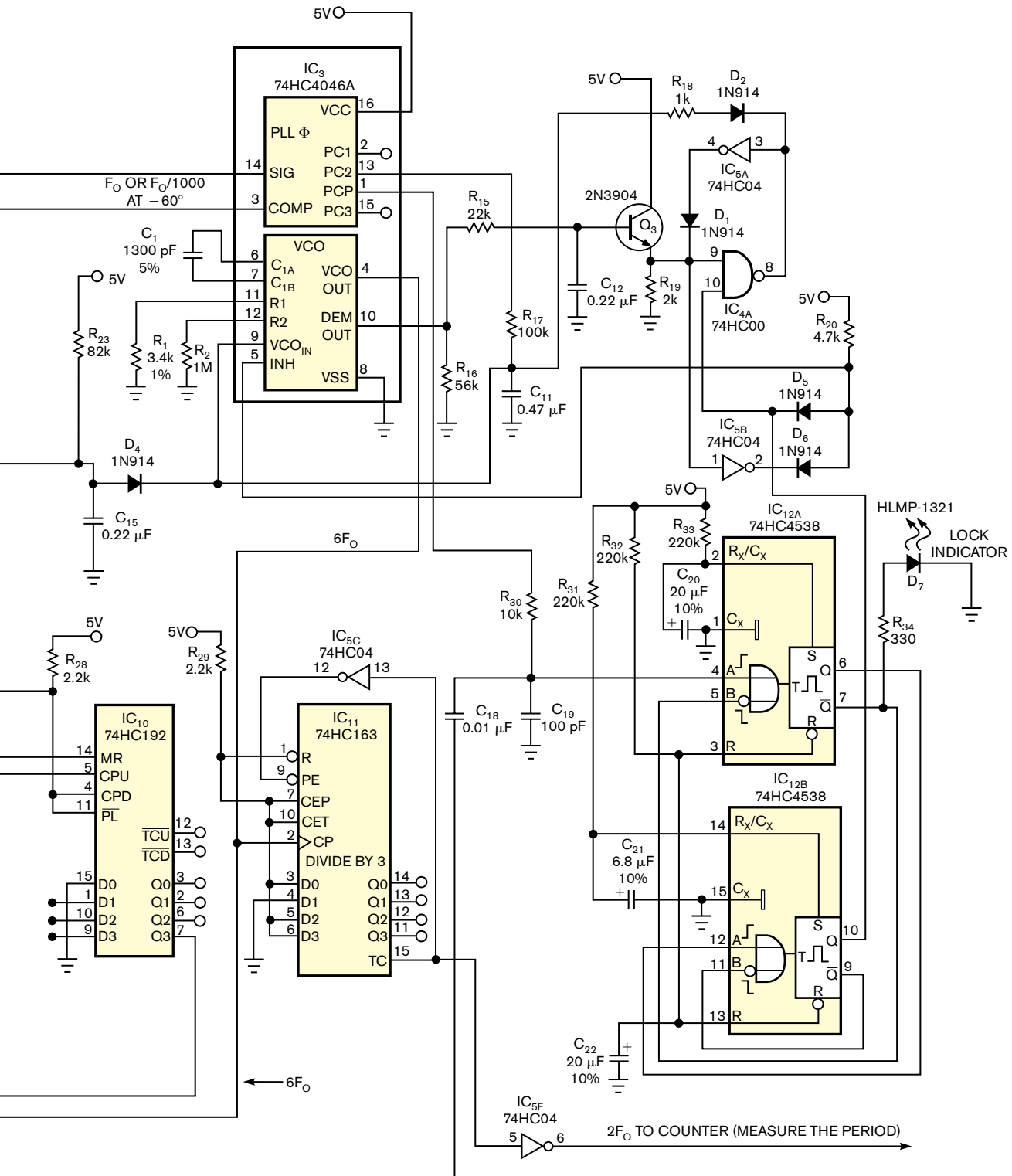
Employing measurements made with the available equipment, which did not include an accurate, high-resolution capacitance meter, this meter is accurate to approximately ±2% over 100 pF to 10 μF (Table 1). The accuracy degrades over 10 to 100 pF because of the input capacitance of the op amp and the associated parasitic capacitance at IC₁'s Pin 3. R₇ and C₆ provide some compensation at the 10- to 100-pF range for the inherent capacitance at that node. R₅ and C₅ provide compensation at the 1- to 10-pF range.

You can also measure the inherent capacitance and then subtract it from the reading on the two lower ranges. If you take this approach, omit R₅, R₇, C₅, and C₆ from the circuit. Then, with S₁ at the 1- to 10-pF range and S₂ at the low-capacitance position, you can measure the capacitance at that node with no external capacitance. The in-

(continued on page 50)

TABLE 1 CAPACITANCE MEASUREMENTS

Range	1 to 10 pF	10 to 100 pF	100 to 1000 pF	1000 to 10,000 pF	0.01 to 0.1 μF	0.1 to 1 μF	1 to 10 μF
Capacitance	5.24, 10.04	10.04, 23.22, 47.6, 102.68	102.68, 469.32, 1022.1	1022.1, 5226.9, 10,140	0.01014, 0.10052	0.10052, 1.034	1.034, 10.07
Measurement error (%)	-8.85, 2.89	6.37, -4.78, -3.68, -0.61	-0.86, -2.5, -0.7	-0.89, -1.28, 0	0.89, 0.88	2.27, -0.87	2.03, 1.24



(continued from page 47)

trinsic capacitance of the test circuit is 2.8 pF. Using this correction, the values you obtain on the lowest two ranges are accurate to approximately $\pm 2\%$, or ± 1 pF.

You must observe capacitor polarity when measuring electrolytic capacitors. Connect the negative end of the capacitor to the grounded terminal. Also, the circuit provides no overvoltage or ESD (electrostatic-discharge)

protection, so be sure to discharge the capacitors before connecting them to the capacitance meter and use an ESD wrist strap to avoid damaging the circuit. For best results, you need accurate and stable 5 and 8V power supplies. Both supplies should be accurate to $\pm 2\%$. You can raise the 8V supply to 9V and relax the accuracy to 5%. If you use a 9V battery to supply the 8V, you can let the voltage drop to about 7.9V before adversely affecting the

performance of the meter. You must, however, maintain the 5V supply at a constant, accurate value. Note that all of the ICs except IC₁ have 0.1- μ F bypass capacitors from their 5V pins to ground. **EDN**

REFERENCE

■ Pyle, Ronald E, "Phase-locked loop aids in measuring capacitance," *Electronics Designer's Casebook*, No. 4, pg 32.

Resistor compensates for instrumentation-amp gain drift

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Some instrumentation amplifiers use external resistors to set their gain. Unfortunately, the lack of temperature-coefficient matching between the external and the internal resistors results in a high gain drift. If, however, another on-chip resistor is available, you can use it to compensate for gain drift as a result of temperature.

As an example, Analog Devices' (www.analog.com) AD8295 has a drift of as much as -50 ppm/ $^{\circ}$ C, even if you use a zero-drift gain-setting resistor. In this Design Idea, you can compensate this drift with an extra zero-drift resistor in combination with an internal chip resistor.

The gain-set equation from the data

sheet (Reference 1) is

$$GAIN = 1 + \frac{49,400}{R_G}$$

From this gain-set equation, you can assume that the chip uses two 24.7-k Ω resistors with the external gain resistor, R_G , to set the amplifier's gain. The chip has two more 20-k Ω resistors. Because all of these chip resistors are of the same magnitude, they probably will have good temperature-coefficient matching, and you can use this matching for compensation. If the amplifier resistance, R_A , and the gain resistor are zero-drift resistors (Figure 1), then

$$GAIN = \left[1 + \frac{49,400(1 + \Delta)}{R_G} \right] \left[1 + \frac{2 \times R_A}{20,000(1 + \Delta)} \right]$$

where Δ is the drift of the internal matched resistors. If

$$\frac{49,400}{R_G} = \frac{R_A}{10,000}$$

then the first-order drift of the gain cancels, and the gain splits equally between the instrumentation amplifier and A_1 . Solving for R_G and R_A yields

$$R_G = \frac{49,400}{\sqrt{GAIN-1}}$$

$$R_A = 10,000 (\sqrt{GAIN-1})$$

For gain greater than 100, the amplifier resistance becomes greater than 90 k Ω , which can be problematic. In this case, you can use A_1 in an inverting configuration with a gain of -1

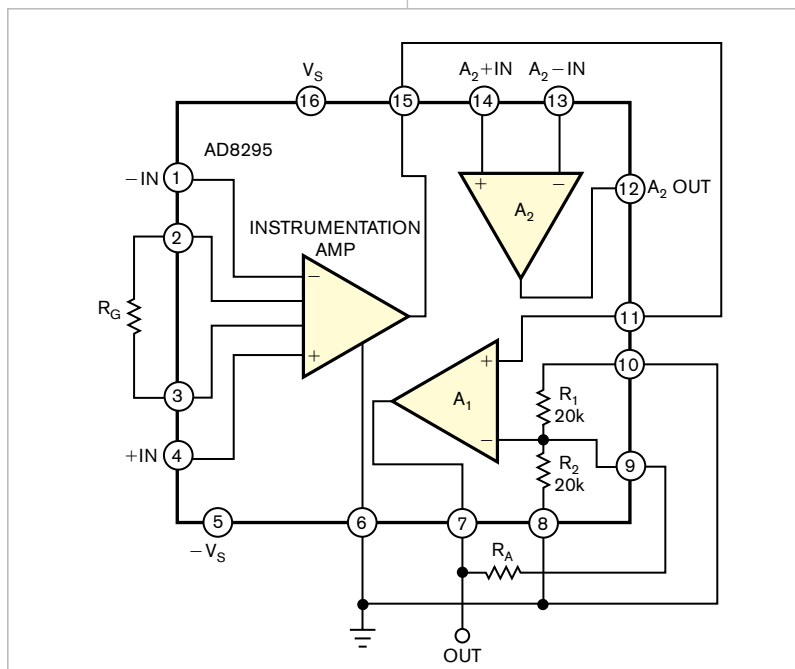


Figure 1 In this configuration, the first-order drift of the gain cancels, and the gain splits equally between the instrumentation amplifier and A_1 .

(Figure 2). With an amplifier resistance of 10 kΩ,

$$\text{GAIN} = \left[1 + \frac{49,400 (1 + \Delta)}{R_G} \right]$$

$$\left[\frac{2 \times R_A}{20,000 (1 + \Delta)} \right] = \left[\frac{1}{(1 + \Delta)} + \frac{49,400}{R_G} \right].$$

This case sizes R_G using a value from the data-sheet formula. If the gain is 50, the internal matching and the negative drift compensate the “49” part of the gain, and the “one” part is just the drift divided by 50 in the total gain, resulting in a typical figure of -1 ppm/°C. In both cases, the resulting gain temperature coefficient can be less than 5 ppm/°C, which is 10 times better than the original outcome. **EDN**

REFERENCE

1 “AD8295: Precision Instrumentation Amplifier with Signal Processing Amplifiers,” Analog Devices, www.analog.com/en/amplifiers-and-comparators/instrumentation-amplifiers/ad8295/products/product.html.

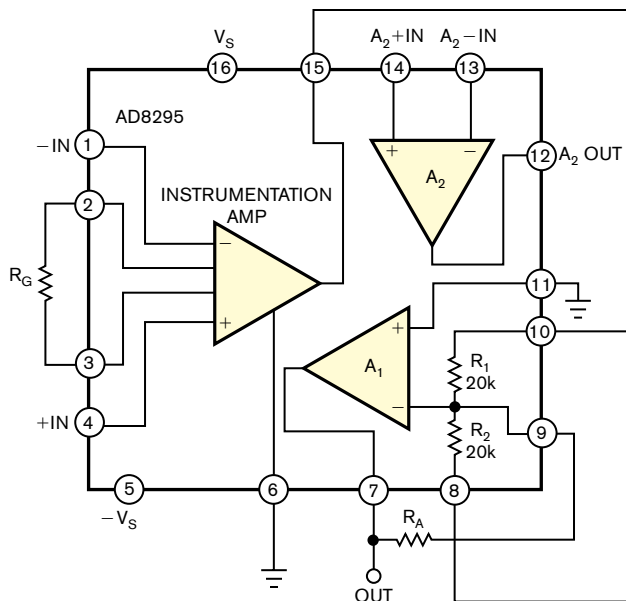


Figure 2 For gain greater than 100, the amplifier resistance becomes greater than 90 kΩ, in which case you can use A_1 in an inverting configuration with a gain of -1 .