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READERS SOLVE DESIGN PROBLEMS

Astable multivibrator gets hysteresis from positive-feedback stage

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Many designs exist for logic-based astable multivibrators, one of the simplest being an RC feedback loop around a single inverting Schmitt trigger inverter (Figure 1). The output charges the capacitor to the upper switching threshold, at which point the output switches to its opposite state, the threshold switches to a different value, and the capacitor's charging current reverses direction. When the capacitor's voltage crosses the lower threshold, the output and threshold both toggle back to their original val-

ues, and the process repeats. The timing depends on both the RC time constant and the hysteresis resulting from the spread between the two threshold values (Figure 2). Unfortunately, although inverter manufacturers specify the hysteresis voltages in their data sheets, the devices have a fairly large range. In addition, they likely have some temperature dependence. These uncertainties make it difficult to design the circuit to have a predictable oscillating frequency.

A simple inverter, without the hys-

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teresis to let it overshoot the nominal threshold, charges the capacitor to the threshold voltage and stops in its narrow linear region. At this point, the

negative feedback from the inverting output to the input regulates the output to the threshold voltage. Adding another inverting stage injects hysteresis of a different form by means of positive feedback, which external passive

TABLE 1 74VHC04 RESULTS

Resis- tance (k Ω)	Timing ca- pacitance (pF)	Hysteresis capaci- tance (pF)	Expected results		Measured results		Total time differential (%)
			Hysteresis voltage (V)	Total time period (nsec)	Hysteresis voltage (V)	Total time period (nsec)	
10	470	100	0.88	3462	0.75	2930	18
10	470	220	1.59	6850	1.8	7340	-7
10	12,000	12,000	2.5	333,526	2.6	364,800	-9
0.3	220	220	2.5	221	1.75	240	-8
1	12,000	12,000	2.5	34,086	2.5	36,000	-5

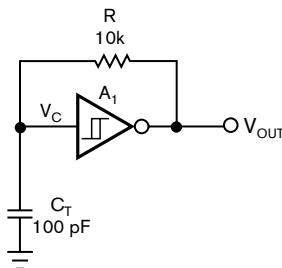


Figure 1 A basic astable multivibrator uses a Schmitt trigger and an RC network.

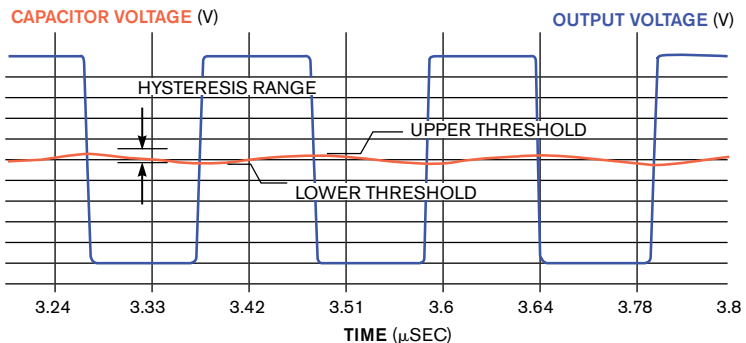


Figure 2 A part's hysteresis, in large part, determines switching thresholds.

parts determine (Figure 3).

Whenever Stage 1 crosses its threshold, the extra Stage 2 injects an additional charge through a feedback capacitor to make the timing capacitor's voltage jump past the threshold. The RC charging current reverses direction to get back to the threshold voltage. When it gets there, the hysteresis-injection circuit again jumps the voltage past the target so that the RC timing circuit must again reverse the charging current to seek the threshold voltage (Figure 4). This process continues endlessly at a fairly predictable rate. In the equations, C_T is the timing capacitor, C_H is the hysteresis capacitor, V_{THRESH} is the threshold voltage, V_{LOW} is the low output voltage, and V_{HIGH} is the high output voltage.

You can view the hysteresis-overshoot voltage, V_{HYST} , as the result of a capacitive voltage divider that timing capacitor C_T and hysteresis capacitor C_H form. When Stage 1 toggles Stage 2, its output jumps from a low value to a high value or from a high value to a low value by an amount of $V_{HIGH} - V_{LOW}$, and the voltage of the timing capacitor jumps by $V_{HYST} = (V_{HIGH} - V_{LOW})(C_H / (C_H + C_T))$. Second, the voltage of the timing capacitor relaxes back toward Stage 1's output voltage by drawing current through both the timing capacitor and the hysteresis capacitor.

Thus, the relaxation time constant is $R(C_T + C_H)$ and the relaxation voltage is either $V_{CT} = (V_{THRESH} + V_{HYST} - V_{LOW}) \exp(-t/R(C_T + C_H))$ or $V_{CT} = (V_{HIGH} - (V_{THRESH} - V_{HYST})) \exp(-t/R(C_T + C_H))$, depending on which half-cycle is occurring. You calculate the time from $V_{THRESH} + V_{HYST}$ back to V_{THRESH} as $t_1 = -R(C_T + C_H) \ln((V_{THRESH} - V_{LOW}) / (V_{THRESH} + V_{HYST} - V_{LOW}))$. For the other half-cycle, $t_2 = -R(C_T + C_H) \ln((V_{HIGH} - V_{THRESH}) / (V_{HIGH} - V_{THRESH} + V_{HYST}))$.

You should add the total propagation time ($t_{PLH} + t_{PHL}$) through stages 1 and 2 to the total period. Unless you want the circuit to operate at its maximum frequency, these propagation times become insignificant. The period pre-

dition then depends only on passive-component values and their tolerances, temperature, and aging coefficients. The series combination of C_T and C_H , however, presents a capacitive load to Stage 2. This load affects Stage 2's rise and fall times, the sum of which you must add to the total period, T.

In the case of CMOS parts, such as the 74VHC04 from Fairchild Semiconductor (www.fairchildsemi.com), rise and fall times depend on the output resistance of the part as well as on the external components. If you model the Stage 2 output as an RC circuit, you can estimate the 10 to 90% exponential rise and fall times as $t_{RISE2} = t_{FALL2} = 2.2R_O(C_T C_H / (C_T + C_H)) + t_O$, where t_{RISE2} is the rise time, t_{FALL2} is the fall time, R_O is the output resistance of the part— 30Ω for the 74VHC04—and t_O is the no-load rise time—in this case, 4.5 nsec for the VHC04. Thus, the total period is $t_1 + t_2 + 2(t_{PLH} + t_{PHL}) + t_{RISE2} + t_{FALL2}$.

Also note that the timing depends on inverter output voltages and the location of the threshold voltage within that range. For example, a CMOS part whose outputs are close to the power rails is more predictable than a TTL (transistor-transistor-logic) part, and a 74HC part with a mid-point threshold voltage has a more symmetric output than an HCT part whose threshold voltage is offset for TTL interfacing.

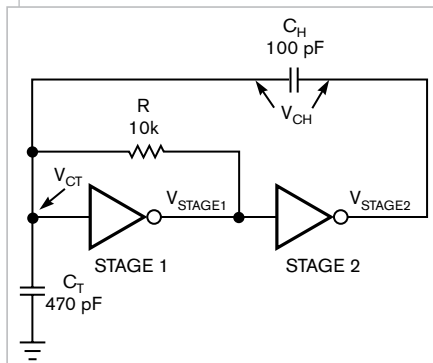


Figure 3 The addition of a positive-feedback stage provides hysteresis to a simple inverter stage.

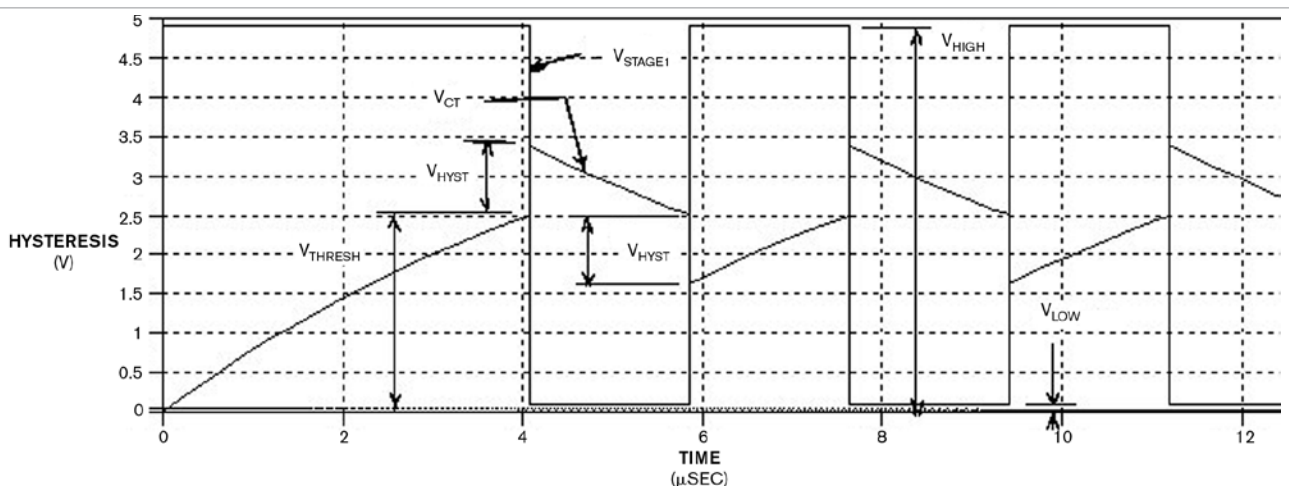


Figure 4 Hysteresis results from a charge burst from Stage 2 that jumps the timing-capacitor voltage past the switching threshold by a known, fixed amount.

For higher frequencies, you must use smaller resistor values, smaller timing-capacitor values, or both. For predictable results, the value of the timing capacitor should be no less than 10 times the inverter's input capacitance, which ranges from 3 to 10 pF for a typical CMOS, and R should not be so low that it significantly loads down the output. As a precaution, the value of the hysteresis capacitor should not exceed that of the timing capacitor so that it does not exceed the maximum input voltage on Stage 1. If the value of the hysteresis capacitor were much greater than that of the timing capacitor, then the threshold voltage and the hysteresis voltage would approach 7.5 and -2.5V, respectively. The 74VHC04 part proves the calculations using 5% resistors and 20% capacitors.

Table 1 summarizes the results, which are within the component tolerances. Figure 5 shows a typical input and output plot. EDN

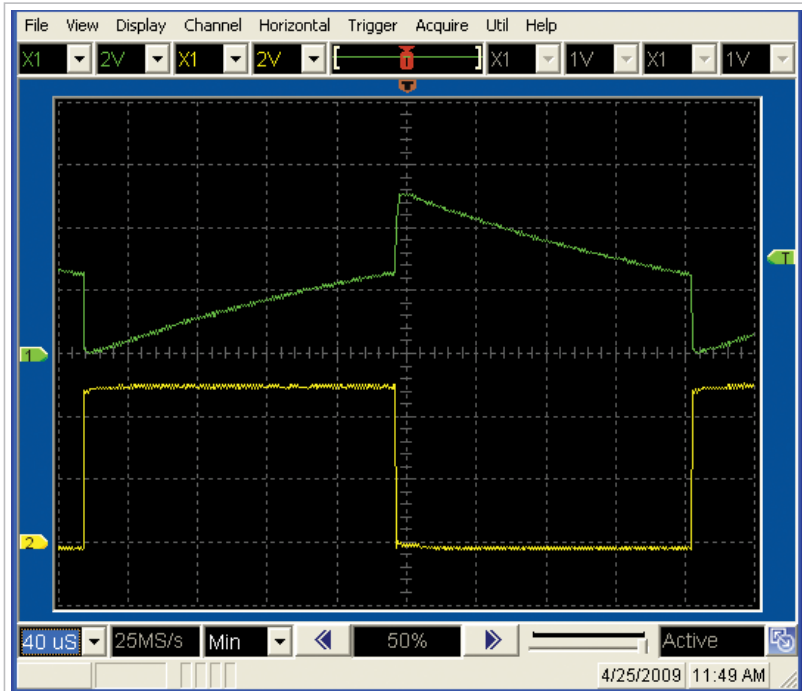


Figure 5 The circuit is well-behaved at low frequencies.

Class B amplifier has automatic bias

Pierre Corbeil, Paradox Innovation, Montreal, PQ, Canada

Class B amplifiers are prone to crossover distortion, which occurs in the output stage in which conduction transfers from one transistor to the other. To prevent crossover distortion, a bias current must flow in both transistors simultaneously. The bias current prevents both transistors from turning off in the transition region. Classic bias circuits keep a constant dc polarization voltage between the bases of the two transistors. Often manually adjusted, it keeps the two transistors on the edge of conduction when there is no signal present. Such a circuit is sensitive to temperature and needs some form of compensation to prevent thermal runaway, which can lead to failure. Figure 1 shows an approach in which automatic bias eliminates the problem.

In this Class B amplifier, R_1 sets the bias current at idle mode with no sig-

nal. Emitter current for Q_3 is $(V_{CC} - V_{BIAS} - V_{BEQ3} - V_{BEQ1})/R_1$, where V_{CC} is the power-supply voltage, V_{BIAS} is the dc voltage on the emitters of Q_1 and

Q_2 , V_{BEQ3} is the base-to-emitter voltage of Q_3 , and V_{BEQ1} is the base-to-emitter voltage of Q_1 . Q_1 and Q_2 mirror this current because Q_1 and Q_3 share the same base current, as do Q_2 and Q_4 . Assuming that the four transistors are perfectly matched, all of them have the same base current and the same collec-

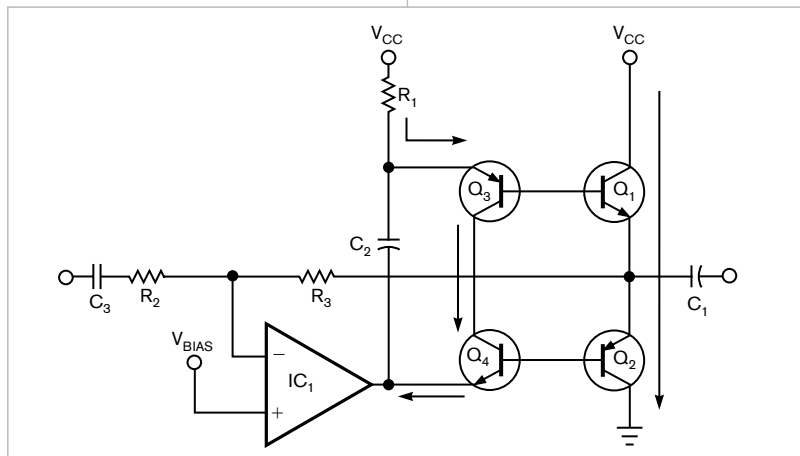


Figure 1 A bias current flows in the transistors that prevents Q_1 and Q_2 from being off simultaneously.

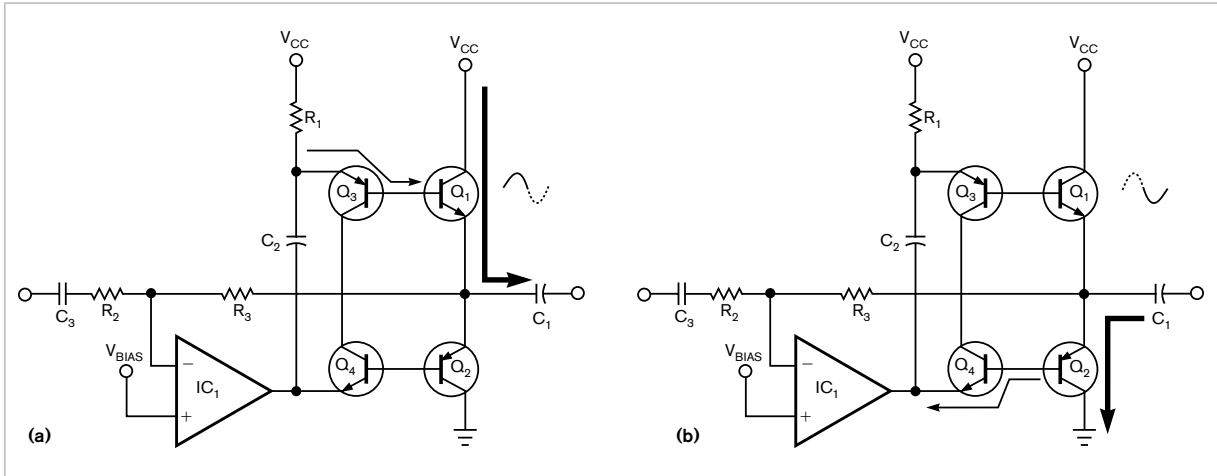


Figure 2 On a positive half-cycle, current flows from Q_1 through C_1 to a load (a). On a negative half-cycle, current flows through Q_2 (b).

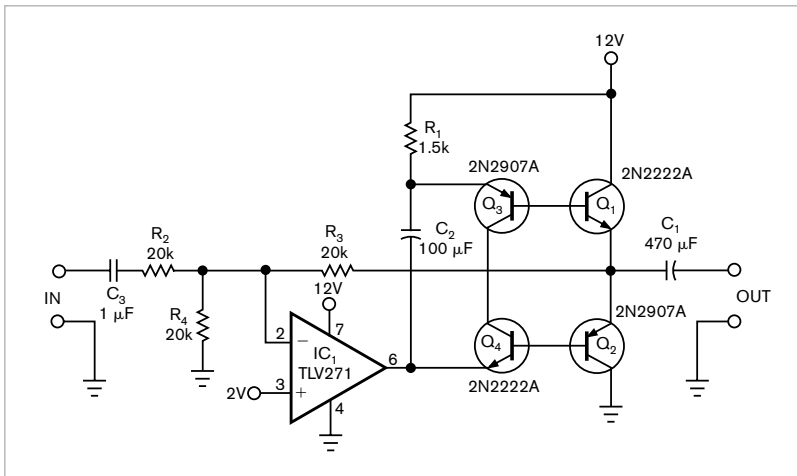


Figure 3 A typical application of this Class B circuit is a headphone amplifier.

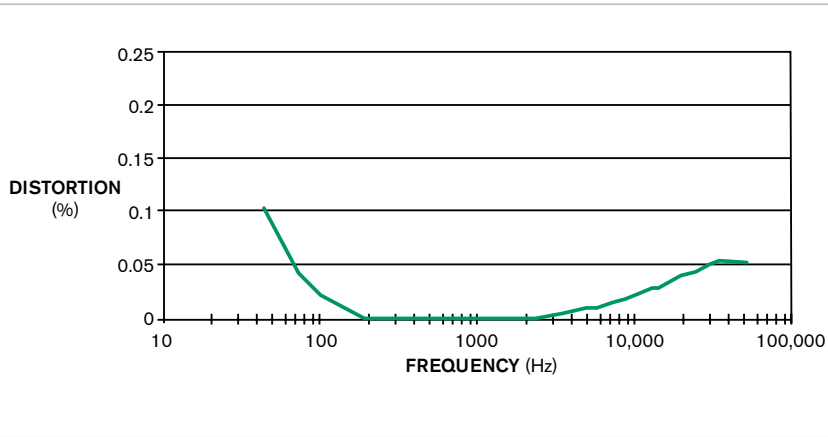


Figure 4 This graph shows distortion as measured on the circuit of Figure 3.

tor current, so the emitters of Q_1 and Q_2 precisely mirror the current in R_1 . Transistor matching is unnecessary, however. With unmatched transistors, either Q_3 or Q_4 must operate in saturation, and, because the mirror effect depends on the transistors' current gain, h_{FE} , the difference between Q_1/Q_2 bias current and the current in R_1 can be significant. This circuit automatically adjusts the voltage on C_2 to compensate for temperature and the transistors' characteristics.

When a signal is present, the current gain is the h_{FE} of output transistor Q_1 or Q_2 (the same as for a classic Class B amplifier). On the positive part of the signal, Q_1 carries the load current. Because the base current increases, Q_3 enters saturation. On the negative part of the signal, Q_2 carries the load current and Q_4 saturates.

Figure 2 shows the ac-current path. The maximum average load current is the idle current in R_1 times the current gain of Q_1 times two. The op amp must be able to sink the base current of Q_2 (load current/ h_{FE}) + $((V_{CC} - V_{BE} \times 4) / R_1)$. A typical application of this Class B amplifier delivers 0.25W into 8Ω (**Figure 3**). **Figure 4** shows the total harmonic distortion over the 45-Hz to 50-kHz band—that is, 1V rms into 8Ω . **EDN**

Cable tester uses LEDs to find faults

Pavel Šádek, Apri, Rožnov pod Radhoštěm, Czech Republic

This Design Idea describes a simple cable-test machine that visually shows continuity issues on a 16-wire cable harness for ultrasonic-parking-aid systems. A subcontractor produces the harness in low volumes, making it impractical to use an automated tester. For simplicity, the test signal drives LEDs for a visual indication of continuity.

The circuit in **Figure 1** generates a

binary number from zero to 15 (0000 to 1111). You can generate the numbers with a 555 timer and a binary counter, but this circuit uses a tiny, eight-pin microcontroller. A four-wire bus sends the digits to two four-to-16-line 74HC154 decoders, which generate active-low signals on their 16 lines. Inverting the outputs of the driver decoder with a 74HC04 inverter provides a drive signal for an LED

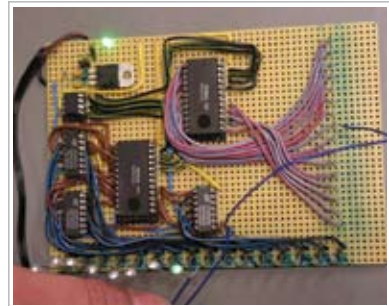
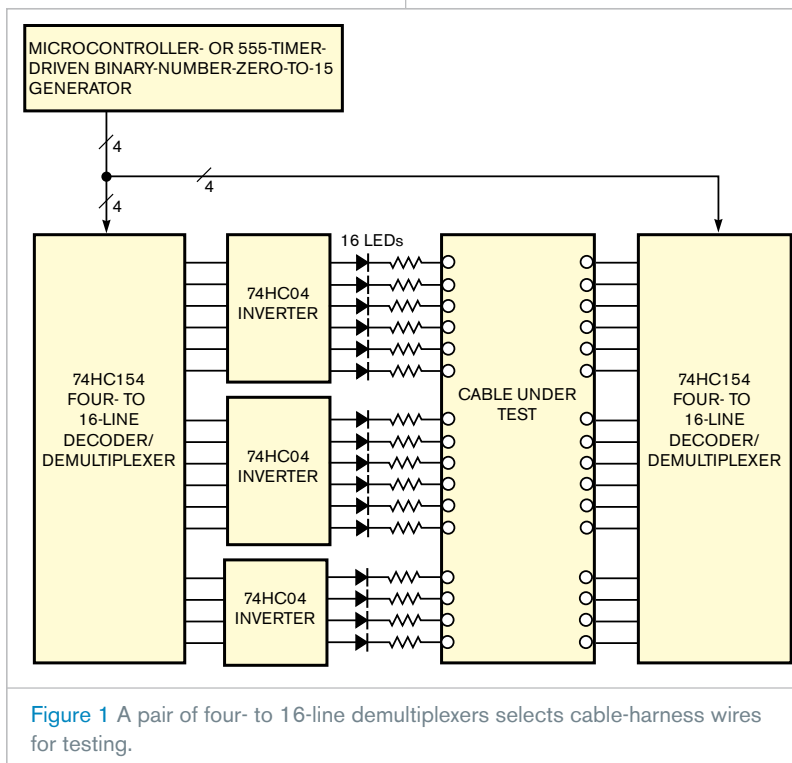


Figure 2 The cable-harness tester uses LEDs to indicate good connections.

and current-limiting resistor on each harness wire.

The tester should produce one and only one illuminated LED for a good wire as the circuit scans the harness. If the scan is fast enough, all LEDs will all appear to be on, although each is on for just one-sixteenth of the time. **Figure 2** shows the completed circuit with eight LEDs, but it has room for 16 LEDs.

Broken wires in a harness, wrong wire positions, or other continuity failures lead directly to the turn-off of the corresponding LED. Swapped wires can also lead to the turn-off of two LEDs. Meanwhile, only one cathode is driven high, whereas the others are driven low, and only the cathode's anode is driven low, whereas the others are driven high. So only correctly connected wires could pass this test.

If you need to test harnesses with more than 16 wires, you can cascade additional decoders. You can also use a high-pin-count microcontroller in the same way. **EDN**

Dual-coil relay driver uses only two MOSFETs

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Latching relays change their states when you apply a short voltage pulse to their coils. Because these relays require no continuous coil currents to keep their states, you can save considerable power in the driver

circuit. In one type of latching relays, you can alternately energize dual coils to change the relay state. Simply apply voltage to one coil for the set state and to the other coil for the reset state. Applying a 25- to 50-msec-wide voltage

pulse to the coils is sufficient for operating the relay. Many relays can operate with a continuous coil current, and some dual-coil relays have internal contacts that interrupt the coil current after it completes a state change. Continuous coil voltages can drive such relays if energy efficiency is not a big concern.

The need to differentially drive the coils results in crowded drive circuits for dual-coil relays. Drivers usually in-

clude logic elements to make sure to energize only one coil at a time. The design in **Figure 1** uses only two MOSFETs to drive a dual-coil RF relay. The Agilent Technologies (www.agilent.com) N1810UL RF switch has dual 24V coils and internal current-interrupting contacts.

When logic input is high, Q_1 conducts and changes the relay state by activating L_1 . The states of the current-interrupting contacts also change. Meanwhile, Q_2 is off because Q_1 pulls down its gate, which avoids fighting between the coils. If you then apply a low signal to the logic input, Q_1 turns off and keeps the L_1 coil inactive. Because R_1 pulls up Q_2 's gate, Q_2 turns on and energizes L_2 . The 1N4007 diodes prevent inductive kickback. The idea is applicable to dual-coil relays with continuously rated coils or with current-interrupting contacts. In the absence of current-interruption contacts, L_1 can serve as a pullup, and R_1 therefore becomes redundant. **EDN**

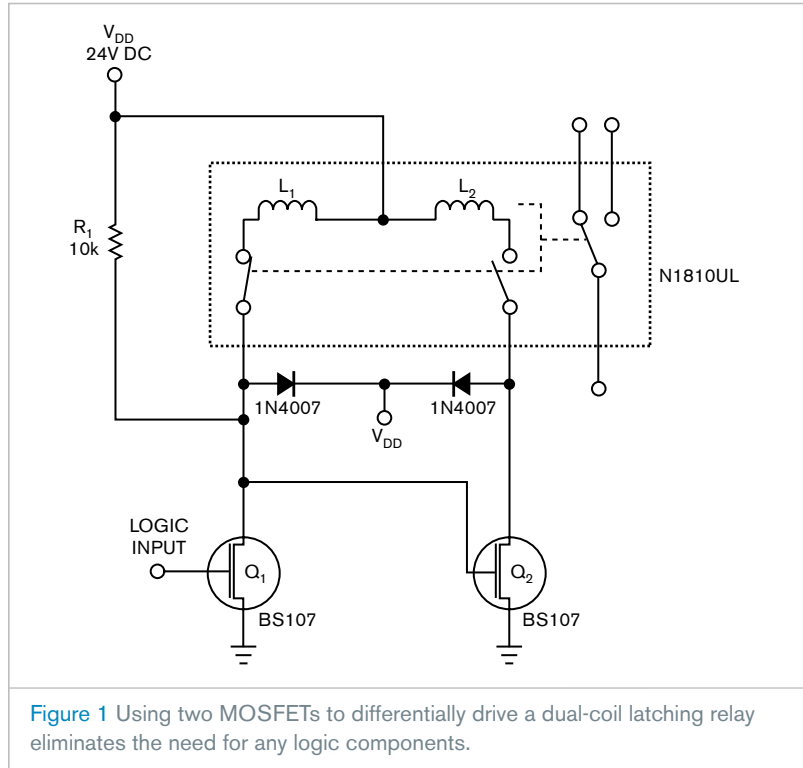


Figure 1 Using two MOSFETs to differentially drive a dual-coil latching relay eliminates the need for any logic components.