EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Negative-to-negative switch-mode converter offers high current and high efficiency

Budge Ing, Maxim Integrated Products Inc, Sunnyvale, CA

When converting a negative-output power supply to one with less-negative output, you must ensure that variations in input voltage don't affect the output voltage. All such supplies include an internal reference voltage that enables output-voltage regulation. You usually refer this reference to the most negative rail, which is ground. Thus, the output voltage of such a converter depends on the accuracy of its negative input supply voltage. The circuit in **Figure 1** lacks that limitation. Delivering output currents as high as 4A with efficiencies better than 90%, it generates a negative output with the help of an op amp and a switch-mode boost converter. Closed-loop feedback regulates the output voltage with respect to ground, the most positive rail,

DIs Inside

46 ADC for programmable logic uses one capacitor

51 Use two phases to cut current and improve EMI

52 Fader switch uses inexpensive controller

▶To see all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

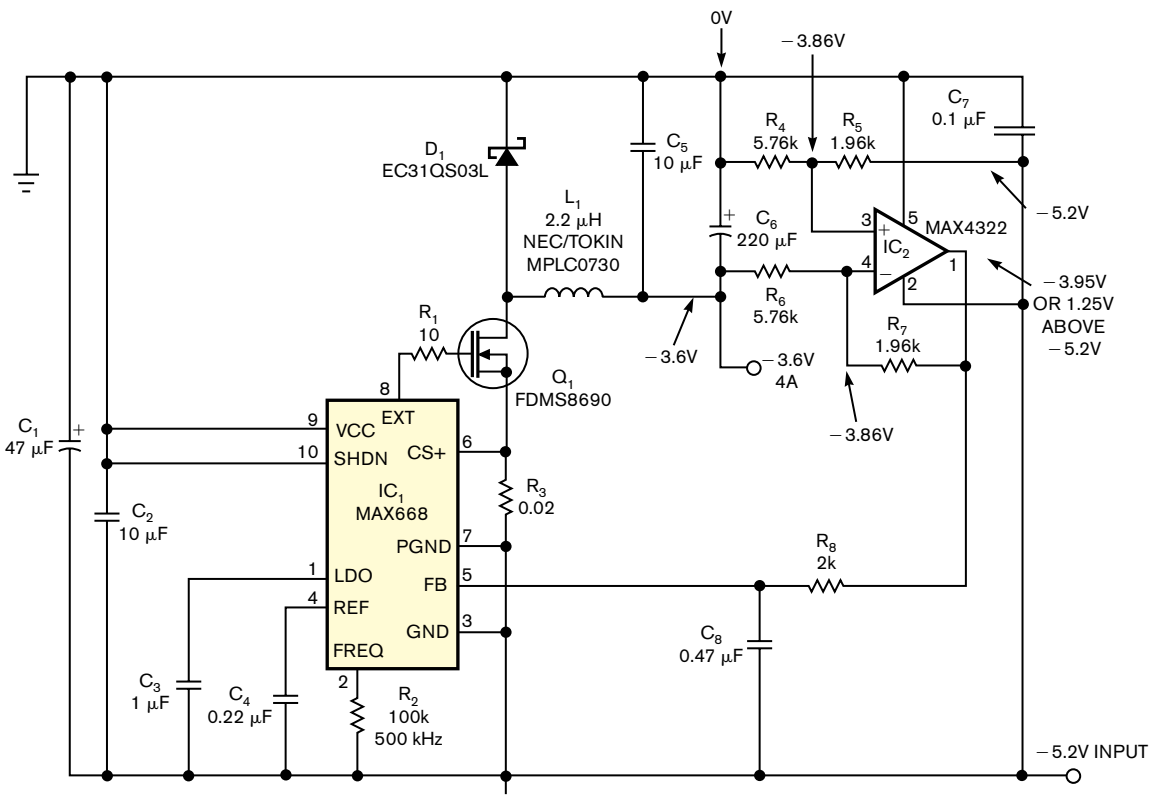

Figure 1 A switch-mode converter generates a regulated negative supply voltage from a more-negative input voltage.

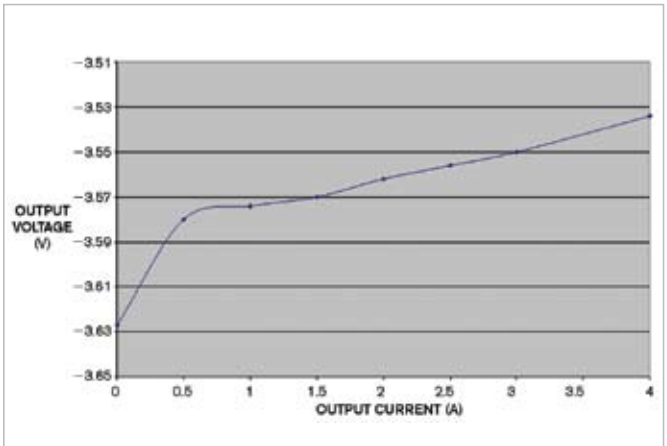

Figure 2 Output voltage for the circuit in Figure 1 varies with output current.

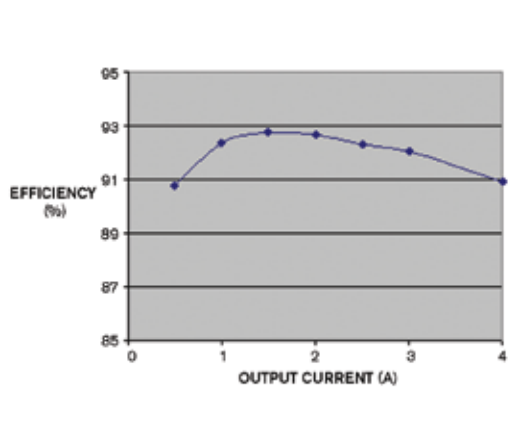

Figure 3 Conversion efficiency for the circuit in Figure 1 varies with output current.

which is also the node from which current is delivered to the load.

The circuit converts a −5.2V supply voltage to −3.6V. The boost converter, IC_1, regulates its output voltage to maintain its feedback voltage at −3.95V—1.25V above −5.2V. Resistor R_8 and capacitor C_8 form a low-pass filter that stabilizes the voltage at FB. You must then select the R_4/R_6 and R_5/R_7 pairs to produce the desired output voltage. Making R_4 and R_5 equal and making R_6 and R_7 equal improves the common-mode performance. The ratio of R_4 to R_5 determines the voltage level at the positive input of op amp IC_2, whose closed-loop configuration ensures that the same voltage appears at its negative input. Knowing IC_2's output voltage, −3.95V, and its negative input voltage lets you determine the output voltage using the values of R_6 and R_7: $V_{OUT}=-V_{REF}(R_6/R_7)$, where V_{REF} is the 1.25V nominal reference voltage of IC_1, $R_4=R_6$, and $R_5=R_7$.

The component values in **Figure 1**—for example, 1.96 kΩ for R_5 and R_7 and 5.76 kΩ for R_4 and R_6—produce an output voltage of −3.76V. Graphs of output voltage versus output current (**Figure 2**) and efficiency versus output current (**Figure 3**) illustrate this circuit's performance. EDN

ADC for programmable logic uses one capacitor

Jef Thoné and Robert Puers,
Katholieke Universiteit Leuven, Leuven, Belgium

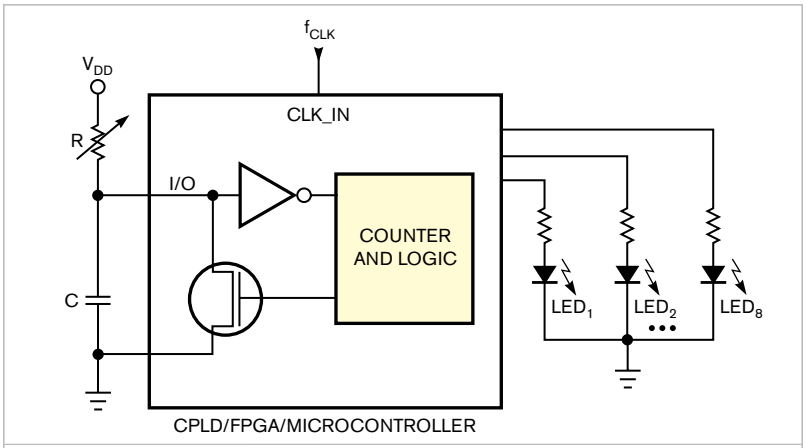

Figure 1 This circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Many electronic devices require user input for setting the application properties. Typical input devices include pushbuttons, potentiometers, and touchscreens. To minimize overall project cost, you may have to select low-range microcontrollers, FPGAs (field-programmable gate arrays), or PLDs (programmable-logic devices). These devices don't provide a wide range of peripherals and often lack analog-to-digital-conversion capability, which can prove annoying when trying to acquire user input. This Design Idea describes a method for adding a low-end ADC to a single programmable-logic I/O pin. The circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Before each measurement, the capacitor discharges to 0V. A single I/O pin can perform both the dis-

charging and the timing. For an FPGA or a PLD, you can perform a discharge by setting the I/O as an output pin and forcing a zero at that pin. You can charge the capacitor by setting the I/O as an input pin, which gives it a high impedance. The capacitor charges through the potentiometer (**Figure 1**). Meanwhile, a counter starts, and the CPLD monitors the input voltage. As soon as the capacitor voltage reaches the threshold, the counter stops at a value that is a measure of the charging time. The charging time or counter value relates to the clock frequency, the value of the resistor, the value of the capacitor, and the input threshold voltage:

Figure 2 The application uses a Xilinx XC9500 XL CPLD.

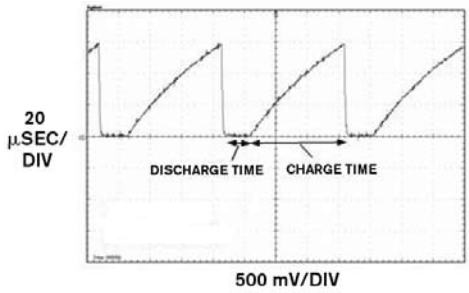

Figure 3 In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor.

$$V_{TH} = V_{DD} \times \left(1 - e^{\frac{-t}{R \times C}}\right)$$

$$T = \frac{COUNTERVALUE}{f_{CLK}}$$

$$COUNTERVALUE = -f_{CLK} \times R \times C \times \ln\left(1 - \frac{V_{TH}}{V_{DD}}\right).$$

If you assume that the capacitor value, the input threshold voltage, and the clock frequency remain fairly constant over the operating range, the charging time is linearly dependent on the value of the resistor. If you replace the resistor with a potentiometer, a counter value depends on the potentiometer position. The application uses a Xilinx (www.xilinx.com) XC9500 XL CPLD (**Figure 2**). The I/O, which VHDL (very-high-speed-IC hardware-description language) declares as a tristate buffer, first shorts the capacitor. Hardware limits the output short-circuit current of the I/O pins to ±10 mA, so the capacitor's shorting should last long enough to guarantee a full discharge. You can calculate the minimum shorting time using the capacitor value, short-circuit current, and discharge voltage, assuming that the threshold voltage must discharge from the capacitor:

$$t_{DISCMIN} = V_{THRESHOLD} \times \frac{C}{I_{SHORT}}.$$

The discharge delay can be realized with a small counter. After the discharge time, the I/O pin acts as an input, which causes the capacitor to charge through a pullup potentiometer. Meanwhile, the internal counter starts. When the capacitor voltage reaches the input threshold voltage, the counter stops. Eight LEDs show the 8-bit value. In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor. The input clock of the PLD is 1.8432 MHz. The input threshold is 1.5V at a supply of 3.3V. This arrangement allows a measurement range between a counter value of 25 and 270, equivalent to a resolution of almost 8 bits. **Figure 3** shows the capacitor charging/discharging waveform.

Every IC's I/O pin has a certain bias sink or source current, causing a voltage drop over the charging resistor. This situation limits the charge voltage to $V_{DD} - R_{CHARGE} \times I_{BIAS}$. In other words, if the charging resistance is too large, the capacitor doesn't charge above the input-pin threshold voltage, stopping the circuit's operation. Similar applications for microcontrollers or PLDs (**references 1** through **5**) include adding multiple inputs to a single I/O pin and using a different pullup-resistor value for each input. By discriminating the charging times for each resistor, the PLD can decide which resistor or combination of resistors the user has actuated.

Another application for microcontrollers is temperature measurement. By replacing the pullup resistor with a PTC (positive-temperature-coefficient) or an NTC (negative-temperature-coefficient) resistor, you can derive the temperature from the charging time after calibration. You can also use these devices to make true analog-to-digital measurements. By replacing the pullup resistor with a voltage-controlled current source, an input-voltage change causes a linear change in the charging time, providing a real analog-to-digital conversion. EDN

REFERENCES

1. Eggers, Torsten, and Thomas Schmidt, "AN10187 Low-cost A/D-Conversion with Philips LPC Microcontrollers," Philips Semiconductors, Oct 4, 2002, www.nxp.com/acrobat_download/applicationnotes/AN10187_1.pdf.
2. "Using an I/O Port Pin as an A/D Converter Input," Holtek, www.holtek.com.tw/english/tech/appnote/uc/pdf/ha0128e.pdf.
3. "AVR400: Low Cost A/D Converter," Atmel, www.atmel.com/dyn/resources/prod_documents/doc0942.pdf.
4. Quiring, Keith, "Implementing An Ultralow-Power Thermostat With Slope A/D Conversion," Texas Instruments, Jan 2006, http://focus.ti.com/lit/an/slaa129b/slaa129b.pdf.
5. "CoolRunner-II Low Cost, Low Power Thermometer for Embedded Designs," Xilinx, Nov 29, 2004, www.xilinx.com/support/documentation/application_notes/xapp438.pdf.

Use two phases to cut current and improve EMI

Goran Perica, Linear Technology, Milpitas, CA

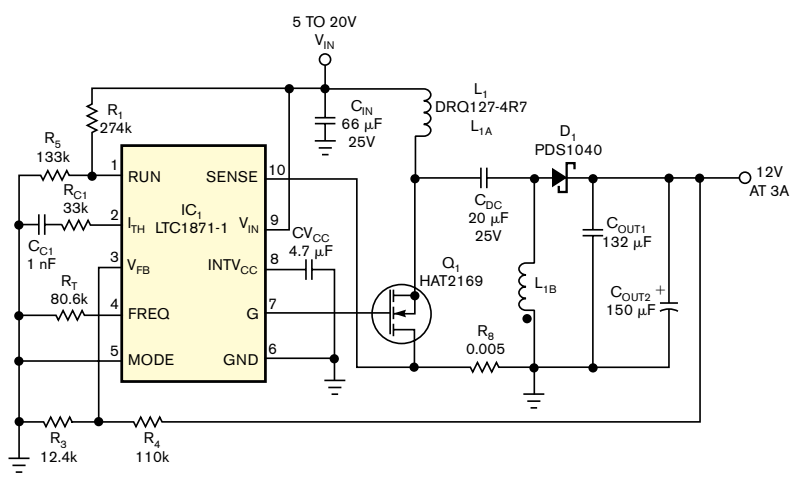

Figure 1 A single-phase SEPIC has low input ripple currents and is suitable for power levels of 5 to 50W.

In dc/dc-converter applications in which the input voltage may be lower or higher than the output voltage, you can use either a flyback converter or a SEPIC (single-ended-primary-inductor converter). SEPICs offer lower input-current ripple and higher efficiency than do flyback designs. Both converters suffer from relatively high output-current ripple, especially at high load currents and low input voltages. As output-current ripple increases, so does the circuit's output-filter-capacitance requirement, which increases size and cost. You can reduce output-current and -voltage ripple without increasing the application size and cost by using a multiphase SEPIC or flyback converter. Using a multiphase flyback circuit also greatly reduces the input-current ripple.

To evaluate the benefits of a dual-phase versus a single-phase SEPIC, this Design Idea compares two designs running at 300-kHz switching frequency. For consistency, both examples use the same power components, resulting in twice the output power in the two-phase design.

The single-phase SEPIC circuit can generate 3A of output current (**Figure 1**). SEPICs are typically 1 to 2% more efficient than flyback converters. **Figure 2** shows the output diode's current (bottom trace) at minimum input voltage and maximum load and the output-voltage ripple (top trace). The circuit's output capacitors must handle the peak output-diode current of 14A. Even though the circuit uses four low ESR (equivalent-series-resistance) output capacitors, output-voltage ripple is still 110 mV p-p. The aluminum output capacitor, C_{OUT2}, doesn't help much in reducing the output ripple due to its much higher ESR. C_{OUT2} mainly helps reduce load transients by adding bulk capacitance to the output rail.

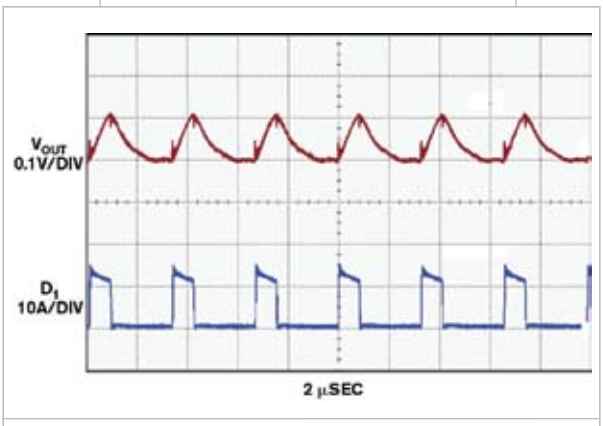

Figure 2 The single-phase circuit in Figure 1 has a peak capacitor output current of about 14A (bottom trace).

Figure 3 (pg 52) shows a two-phase converter, which is similar to the single-phase converter in **Figure 1** except for the addition of an identical second-phase power stage. The second phase halves the peak inductor, MOSFET, and output-diode currents. The 50% lower peak output-diode currents produce 50% lower output ripple (**Figure 4**, pg 52). Also, the output-ripple-current frequency doubles, thus making it easier to filter out with an additional LC filter if necessary.

The benefits of using a dual-phase converter become clear when you consider output-capacitor ripple current (**Figure 5**, pg 52). The two-phase converter's output-capacitor ripple current is always lower than that of an equivalent single-phase converter. Depending on the duty cycle, the two-phase converter's output-capacitor ripple current can approach 0A at a 50% duty cycle. Inductor ripple current is still present, and you can reduce it by using larger inductors.

Using a two-phase converter means that you can use smaller inductors, MOSFETs, output diodes, and output capacitors than you can use in an equivalent single-phase converter. Because high-power designs may need to use more than one MOSFET anyway, a dual-phase design may need only one additional smaller inductor and one smaller diode. Output LC filters can also be smaller because of the doubling of the output ripple frequency. Finally, the EMI performance of a dual-phase SEPIC should be better than that of a single-phase converter because of lower current slew rates and smaller current loops. EDN

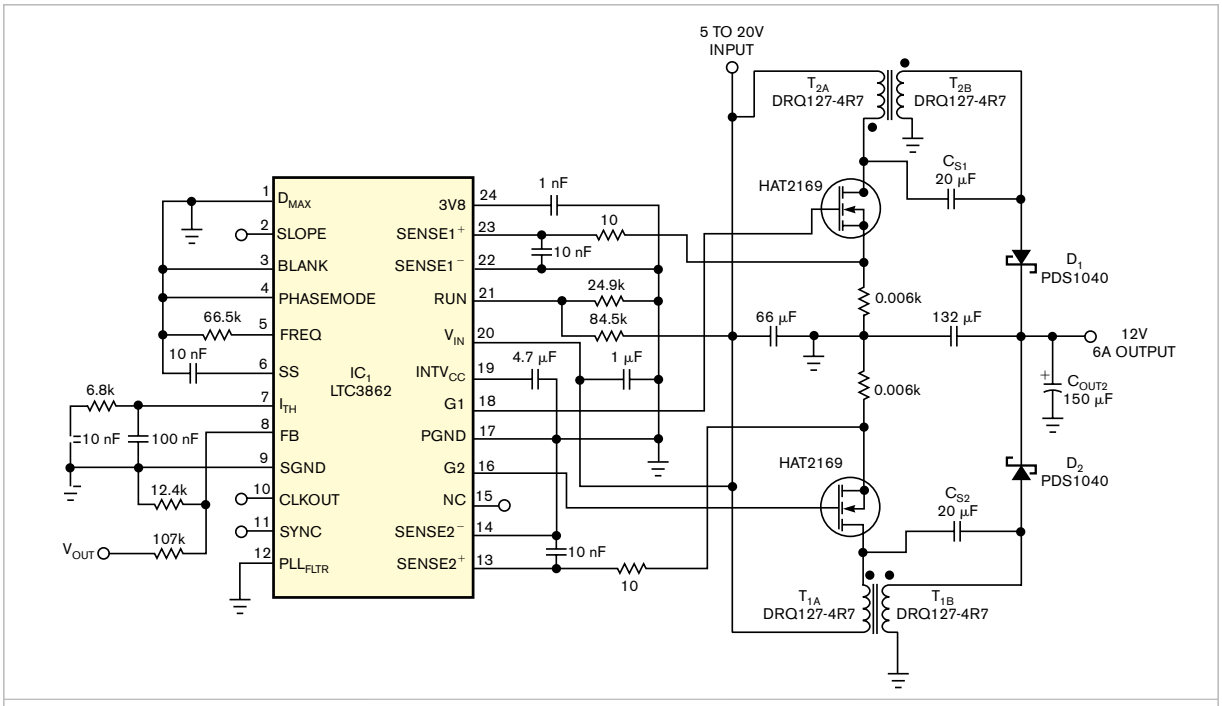

Figure 3 By adding second power stage and shifting the phase by 180°, you can reduce the output ripple currents by more than 50%.

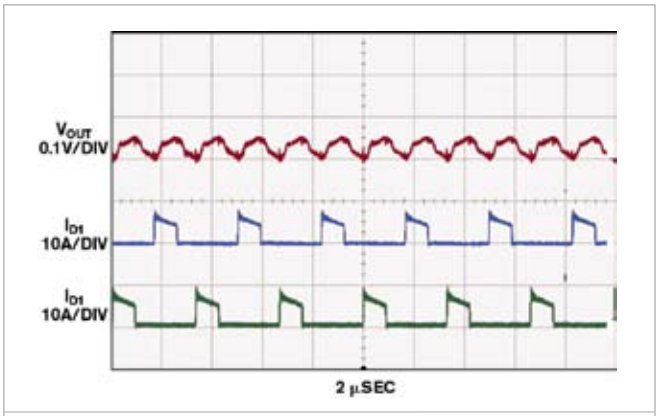

Figure 4 The output ripple current is 50% lower for a two-phase SEPIC. The output ripple voltage is 50% lower than that of a single-phase design with the same output capacitors.

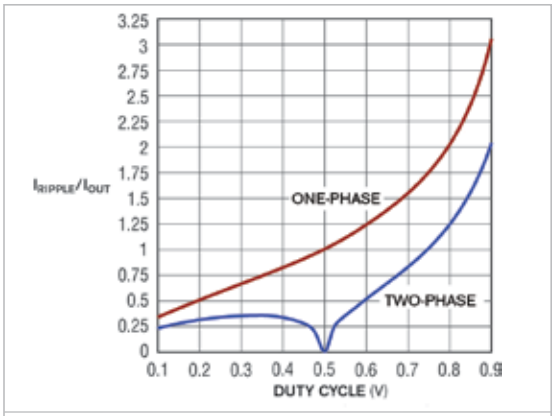

Figure 5 The normalized output-capacitor ripple current for single- and dual-phase SEPICs shows lower output ripple with a two-phase design.

Fader switch uses inexpensive controller

William Grill, Lenexa, KS

Customizing a model or a simulator with a bit of illumination is a nice touch. Rather than a simple on or off, you can add a touch of both refinement and control to your display with fading light. Employing a Microchip (www.microchip.com) 10F20x microcontroller, the circuit in **Figure 1** provides dual-rate fader control for a push-on/push-off switch, a momentary pushbutton switch, or a simple on/off SPST (single-pole/single-throw) switch. The circuit monitors and debounces the switch and generates a multiple-cycle, 470-Hz, PWM (pulse-width-modulated) output to drive LEDs or incandescent lamps. The circuit includes a MAX16823 (www.maxim-ic.com) IC that drives multiple LEDs.

The microcontroller produces 64 linear steps of a PWM signal between 0 and 100% duty cycle. The controller maintains each pulse width for a variable number of cycles employing a table in the assembly code (**Listing 1**,

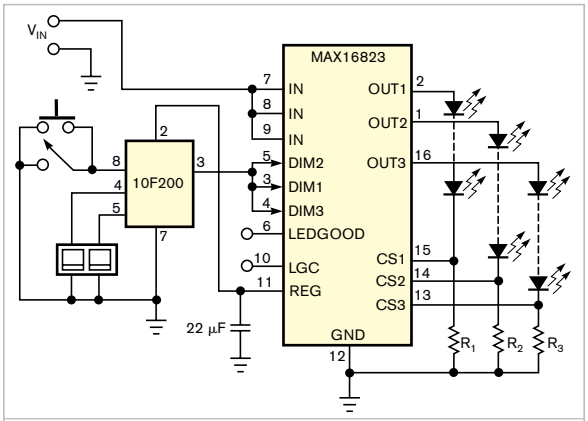

Figure 1 A microcontroller provides pulses with adjustable widths to create fading in LEDs.

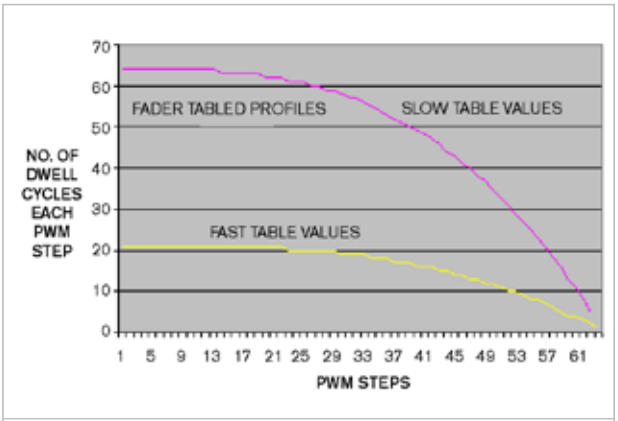

Figure 2 A table in the microcontroller code lets you run fast- or slow-fading profiles.

which you can download at the online version of this Design Idea at www.edn.com/091112dia). You can modify the code to build profiles of LEDs or incandescent lamps by applying a settable dwell time to each PWM step. The code contains two tables to set fast- and slow-fade characteristics. The fade values provide a cubed index that produces a 3-to-1 fade ratio (**Figure 2**). Using the final state of the output at Pin 3 of the 10F200, you access the tabled number of dwell cycles from the first table entry to the last for a high final state or from the last entry to the first to arrive at the final low state.

Fade-transition timing is user-selectable for either a 3- or a 9-second period. The circuit periodically samples both the fade rate and button or switch mode, allowing you to multiplex the design or use it in multiple configurations. The mode control is on Pin 5 of the controller, and the rate control is on Pin 4. The application exploits the controller's internal 4-MHz clock and the configurable pullup resistors on the monitored inputs. A prototype of the circuit uses a 10F20x in an eight-pin DIP, but the controller is also available in a smaller SOT-23 package. EDN