



BY BONNIE BAKER



# Jitter and the ins and outs of SNR

**W**hen you use a high-speed ADC, you expect the performance to meet the published data-sheet SNR (signal-to-noise-ratio) value. When you test the ADC's SNR, you might attach a low-jitter clock device to the converter's clock pin and apply a reasonably low-noise input signal. Several sources of noise errors can cause your converter to fail to meet the publisher specs.

If you are certain that you have a low-noise input signal and a good layout, the combination of the input-signal frequency and the jitter from your clock device is probably the cause of the problem. You will find that low-jitter clock devices are adequate for most ADC applications. However, if both the input-signal frequency to the ADC and the converter's SNR are high, you may need to improve your clock circuit.

Low-jitter clock devices, at best, have advertised 1-psec jitter specifications, or you can generate an equally inferior clock signal from an FPGA. Is-

...sues that contribute to the SNR error of your high-speed ADC include ADC quantization noise, DNL (differential-nonlinearity) effects, the converter's effective internal input noise, and jitter. You can determine whether jitter is the problem by using the following **equation**, which provides the ADC's SNR error that the external clock and ADC jitter exclusively generate:  $SNR_{CLK} = -20\log_{10}(2\pi f_{IN} \times t_{JITTER-TOTAL})$ , where  $f_{IN}$  is the input signal's frequency to the converter and  $t_{JITTER-TOTAL}$  is the rms jitter from the clock signal and ADC clock's input circuitry. Note that  $f_{IN}$  is not the clock frequency ( $f_{CLK}$ ). A

jitter of 1 psec from the external clock to the ADC is adequate for some but not all high-speed ADC applications (**Figure 1**).

The **equation** allows you to calculate an estimate of the required clock jitter for a given ADC. For instance, with an ADC with a specified 70-dB SNR and a 100-MHz in-

put signal, you can calculate the value of  $t_{JITTER-TOTAL}$  as 503 fsec. If the input ADC's aperture jitter is 150 fsec, you can make a high estimate of the external clock-jitter requirements with the following **equation**:  $t_{JITTER-CLK} = \sqrt{(t_{JITTER-TOTAL})^2 - (t_{JITTER-ADC})^2}$ , where  $t_{JITTER-CLK}$  is the jitter that the clock injects into the ADC and  $t_{JITTER-ADC}$  is the ADC's aperture jitter, clock amplitude, and slope. Continuing with the estimate, make  $t_{JITTER-ADC}$  equal only to the ADC's internal jitter of 150 fsec and ignore the effects of the clock amplitude and slope. Using this **equation**, a high estimate of  $t_{JITTER-CLK}$  is 480 fsec.

This column only scratches the surface of the issues behind perfecting the clock signal to a high-speed ADC. You need to give further attention to the clock amplitude and slope because they affect the system jitter. Additionally, you must understand how to implement the hardware portion of a low-jitter clock circuit.

For your next clock design, remember that clock jitter affects the ADC's SNR performance in input frequency to the ADC and the actual clock jitter. Additionally, be skeptical of clock-device vendors' claims. Use the evaluation board from the ADC vendor to test your clock sources before you develop your product. You will be happier with the end results.**EDN**

## REFERENCES

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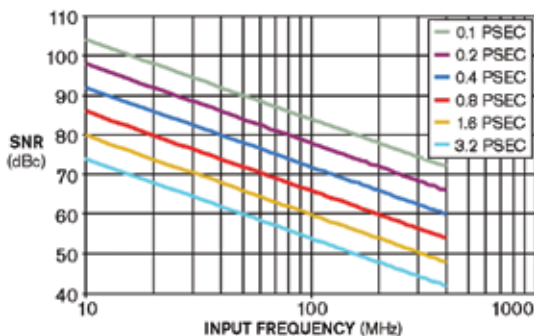


Figure 1 The SNR due to jitter is a function of the input signal's frequency.