

TABLE 2—ACTEL VARICORE FAMILY MEMBERS

Device	PEG array	ASIC gates	Functional groups	Registers	Logic cells	Available I/O	RAM blocks	RAM bits
V18L2x1	2×1	5000	128	512	1024	448	0	0
V18L2x2	2×2	10,000	256	1024	2048	640	0	0
V18L4x1	4×1	10,000	256	1024	2048	704	0	0
V18L4x2	4×2	20,000	512	2048	4096	896	0	0
V18L4x4	4×4	40,000	1024	4096	8192	1280	0	0
V18L2x2R	2×2	10,000	256	1024	2048	640	Four	36,864
V18L4x2R	4×2	20,000	512	2048	4096	896	Eight	73,728
V18L4x4R	4×4	40,000	1024	4096	8192	1280	Eight	73,728